

Questa is the industry-leading verification platform and features the most comprehensive SystemVerilog support and new Verification Management capabilities that link the verification plan to coverage results.

### High-Performance Verification Environment

The Questa™ advanced verification environment from Mentor Graphics® combines high performance and high capacity with the most comprehensive verification capabilities in the industry. Assertion-based verification (ABV), testbench automation, and coverage-driven verification (CDV) are supported natively through Questa’s high-performance assertion engine, a modern, high-performance constraint solver, and extensive functional coverage features, including Verification Management leveraging the Unified Coverage Database (UCDB). Verification of low power design functionality can now be proven with in an RTL environment with Power-Aware Simulation. This full set of advanced verification functionality is enabled by a flexible architecture that delivers unrivaled language and feature support.

Questa works within any design and verification flow, incorporates best-in-class technologies, and spans the levels of abstraction required for complex SoC design and verification. Questa significantly increases the productivity and predictability of any verification methodology while improving design quality, equipping design and verification teams to meet schedules and attain maximum design functionality.

### Major product features:

- Support of object-oriented, class-based verification methodologies, including the Mentor Graphics Advanced Verification Methodology (AVM)
- Built-in Power Aware Simulation enables RTL verification of low power designs
- Native support of all standard languages; including SystemVerilog, SystemC, VHDL, Verilog, PSL, and C/C++
- High-level design with SystemVerilog and SystemC, including multi-language transaction-level modeling and viewing
- Testbench automation with high-performance, constrained-random stimulus generation
- Improved verification quality with Verification Management
- Assertion library support through Accellera OVL and Questa Verification Library (QVL) of advanced checkers and standard protocol monitors
- Industry-leading RTL and gate-level performance
- Powerful, intuitive multi-language GUI speeds analysis of advanced verification languages
- Customizable and open architecture through C and Tcl/Tk interfaces
- UNIX, Linux 32 and 64 bit, and 32 bit Windows-based platform

## Advanced Verification Methodology

Through its comprehensive support of SystemVerilog, SystemC, and the SystemC Verification (SCV) and transaction-level modeling (TLM) libraries, Questa enables the adoption of the Mentor Graphics Advanced Verification Methodology (AVM). The AVM’s “best practices” approach significantly reduces the barriers to successful adoption of object-oriented, class-based verification techniques.

These techniques often involve multi-language verification as members of a project team often employ different languages at different levels of abstraction or for specific tasks. Design and verification engineers need a tool and methodology that allows them to choose the most appropriate language for their particular task.

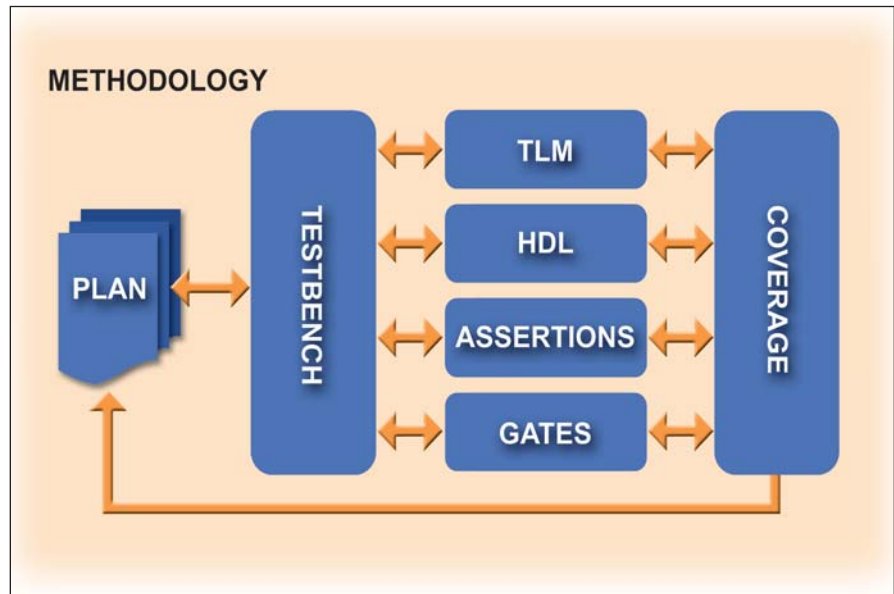
Through the single-kernel, mixed-language environment provided by Questa, the AVM testbench can be connected to designs in Verilog, VHDL, SystemVerilog, SystemC, or any combination thereof. This unparalleled flexibility allows all design and verification teams to quickly gain significant return on investment.

Adopting AVM with Questa closes the chasms between system designers and architects and between RTL designers and verification engineers. It facilitates the design and verification flow from system design to gate-level verification by exploiting the appropriate design and verification language at each step of the project.

Questa supports assertion-based verification, constrained-random testing, and coverage-driven verification at all abstraction levels, so the full benefit of advanced verification can be realized during system design as well as RTL implementation.

The AVM promotes the creation of reusable testbench components based on an open library of parameterized, abstract classes and utilities. Well-defined interfaces — based on the industry standard Open SystemC Initiative (OSCI) TLM library, implemented in SystemC and SystemVerilog — allow each component in the verification environment to be easily reused and modified without impacting other components.

The AVM fully exploits Questa’s inter-process communication capabilities, permitting users to create blocking and non-blocking communication channels between components.



*The ability to efficiently support the different verification methodologies is built into Questa. With native support of assertions, constraints, and functional coverage Questa enables an optimized verification flow that fosters verification predictability and design quality.*

Truly native support of SystemVerilog verification capabilities — such as program blocks, virtual interfaces, and classes — provides the ultimate in flexibility for constructing complex, powerful verification environments, designs at the transaction and register transfer levels, and the connectivity between both design and verification components.

### Testbench Automation and CDV

Questa’s verification features enable the automatic creation of complex, input-stimulus combinations that are extremely difficult to create manually. Stimulus scenarios can be described in terms of constraints using SystemVerilog and SCV library constructs. These constrained-random features help promote reuse at the testbench level, thereby reducing the number of testbenches that need to be written while increasing the amount of tests generated, bugs exposed, and verification coverage achieved.

Questa combines functional coverage with constrained-random testing to identify the functionality exercised by automatically generated stimulus. Using functional coverage metrics as feedback for test creation, engineers can apply constraints to focus random testing on unverified functionality. This automation methodology offers huge productivity improvements over handcrafting hundreds of directed tests. Functional coverage metrics are provided using the Property Specification Language (PSL) cover directives as well as SystemVerilog cover groups and cover directives. Furthermore, testbenches are able to react dynamically to

functional coverage points in the design. As these functional coverage points are detected, the inputs to the constraint solver can be dynamically modified to re-target previously uncovered functionality.

Questa implements CDV and constrained-random test generation in a complementary fashion to improve productivity and predictability. In testbench automation, the random nature of constrained-random testing allows the generation of stimuli and scenarios that may not have otherwise been considered. That randomness in the generation of stimulus requires a method of measuring what has been exercised and what has not. CDV provides that method.

### Verification Management

The application of constrained-random stimulus and CDV dramatically increases the amount of information generated in the verification process. Questa's UCDB collects all coverage data — code coverage, functional coverage, and assertion coverage — into a single database. The Verification Management feature imports verification plans and correlates coverage to test objectives delivering a powerful tool for managers and engineers to continuously track progress and efficiently deploy resources.

Questa provides powerful analysis utilities that process the raw coverage data into actionable information. For example, test ranking identifies redundant tests that provide no net increase in coverage, and it prioritizes tests based on the coverage they achieve. Because many verification flows

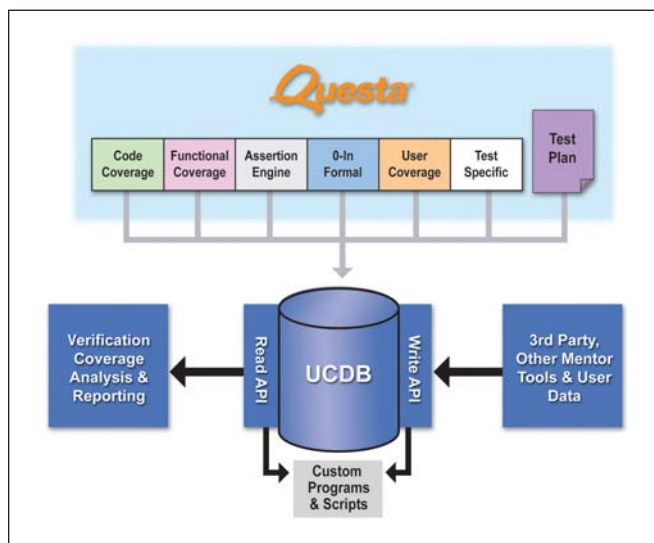
include tools from multiple vendors and verification analysis metrics may be project or organization specific, the Questa UCDB defines a read and write API to the UCDB. Coverage data from proprietary and third-party tools can be inserted into the UCDB through the write API. Custom, proprietary analysis algorithms can be built on top of the read API.

### Assertion-Based Verification

Questa delivers the most comprehensive standards-based ABV solution in the industry, offering the choice of SystemVerilog, PSL, or both. To ease the adoption of ABV, Questa includes SVA, PSL, and Accellera OVL assertion libraries as well as the new Questa Verification Library that contains advanced checkers and standard protocol monitors for AMBA AHB, AXI, OCP, PCI-EXPRESS, USB, Ethernet, and more. Questa integrates ABV with both testbench automation and CDV for a complete, advanced verification environment. ABV makes assertions a key element of verification, ensuring that design properties are not violated. Through its support of all standard, non-proprietary verification and assertion languages as well as multiple verification engines (including simulation, formal verification, and emulation), Questa maximizes the benefits of assertions throughout the verification flow, increasing verification and debug productivity, enhancing design quality, and improving the predictability of verification results.

Because assertions improve observability, design errors are detected at or near their source, as they occur, vastly improving debug productivity. Questa's built-in PSL and SystemVerilog assertion browser, with its assertion debugger, identifies the event that most likely caused an assertion failure and directly traces the offending signal back to the source code. This dramatically improves the time to analyze and fix the root cause of failures. On real-world designs, Questa's native ABV debug environment has reduced the time it takes to trace back and fix a bug from two days to two hours.

Assertions can also be used in conjunction with coverage measurements to increase verification efficiency. The Questa ABV solution accelerates verification closure through coverage metrics specified in SystemVerilog and PSL. The UCDB captures coverage data from PSL and SystemVerilog cover directives. Cover directives capture control coverage (sequences of events), while SystemVerilog covergroups efficiently capture coverage of data values. This data aids in creating tests that will improve functional coverage and design functionality. Questa integrates advanced code coverage with structural, transaction, and functional coverage data collected using assertions, providing immediate feedback on the quality, completeness, and effectiveness of verification.



The Questa 6.3 Verification Management enables users to know when verification coverage goals are achieved. Integrated tools merge, analyze, and report all coverage data from multiple tools in a single database.

## High Performance

The foundation of Questa's industry-leading performance and capacity is the natively compiled single kernel architecture. Support of all languages in a single kernel and single timing wheel establishes the ideal platform for performance. Questa's high-performance global optimization mode, known as vopt, engages very aggressive compile and simulation optimization algorithms for all languages. The vopt performance mode can improve Verilog/SystemVerilog and mixed VHDL RTL simulation performance by up to 6X versus an unoptimized mode. The vopt flow can also improve gate-level performance by up to 4X and capacity by over 2X. Questa's native SystemC integration eliminates performance bottlenecks inherent in PLI or FLI integrations, significantly improving total simulation times.

## Power Aware Verification

Low power management is critical for many applications. The techniques required to manage low power present unique design and verification challenges, including power gating (or power domain on/off), state retention and restoration, and corruption. Typically the verification of this functionality is done ad-hoc by inserting power network functionality into a changing RTL environment, or it is performed late in the design cycle upon the post-layout netlist.

Questa's Power Aware Functional Verification ensures that the power network matches silicon functionality. Raising the abstraction level at which the power network can be verified to the RTL provides the best performance throughput and earliest analysis and debug. There is no impact to either the existing RTL flow or the RTL code because Questa employs a side file to describe the power network. Questa's power aware verification is proven technology that has contributed to successful, low power SoC tapeouts.

## Integrated Multi-Language Debugging

Questa's simulation debug mode is the industry's highest productivity debug environment. The simulator provides a unified kernel for Verilog, SystemVerilog, VHDL, and SystemC with TLM waveform viewing and analysis for authentic multi-language debugging. A fully integrated debug environment supports SystemVerilog along with an assertion debugger. There is no learning curve with the SystemC implementation, since the full-featured, built-in C debugger works on SystemC and HDL code in the same way.

The easy-to-use Questa GUI is the industry's leading graphical interface and makes efficient use of desktop real estate. The logical arrangement of interactive elements makes it easy to view and access Questa's many capabilities. Integration of all language features improves productivity. A memory viewer makes it easy to observe and modify the contents of a design's memory.

## Scalable Verification™

The Questa platform serves as the foundation for Mentor's verification technologies and integrates with other Mentor Graphics products to create customized solutions for specific methodologies. Hardware designers and verification engineers can include embedded software blocks as part of their verification environment. The ability to import firmware quickly, for use as a testbench, boosts verification coverage and accelerates simulation. A transaction-level interface between Questa and Mentor emulators, allows fast simulation execution of design models stimulated using transaction-level testbenches. Verification of digital and analog/digital designs ensures superior accuracy and performance.

Visit our web site at [www.mentor.com/fv](http://www.mentor.com/fv) for the latest product news.

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