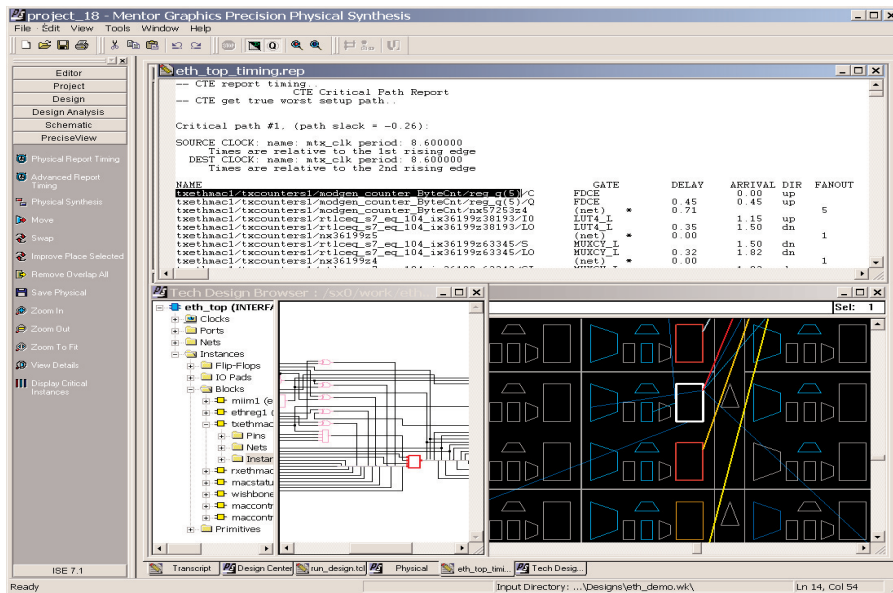


Precision Synthesis



Precision Synthesis is the industry's foremost FPGA design solution, offering ease of use, high-productivity flows and outstanding QoR within a complete vendor-independent design methodology.

Multi-Vendor, Physically Aware FPGA Synthesis

FPGA designs have become increasingly challenging. Incremental design methodologies are needed to effectively manage complexity, reduce risk and accelerate time to market. Moreover, it has become very important for designers to fine-tune FPGA implementations and thus ensure that their challenging designs meet technical and business requirements.

"Push-button-only" flows fail to provide efficient reuse and adequate implementation control to reliably meet design goals. They ultimately limit a design team's ability to consistently bring differentiated products to market.

Combining out-of-the-box ease-of-use, high-productivity design flows and industry-leading quality of results (QoR), even for the most advanced FPGA devices, Precision® Synthesis provides excellent design analysis capabilities and outstanding physical implementation and timing control -- all within a truly vendor-independent design methodology.

Start Designs Right

• Intuitive Graphical User Interface

- + Simple design flow aids new users
- + GUI-based assignment of properties/constraints on selected design objects
- + Provides instant access to all design-related data files

Key Product Features:

- **Integrates Powerful RTL Synthesis with Advanced Physical Optimization Flows**
- **Start Designs Right**
 - Provides superior support for SystemVerilog, Verilog and VHDL
 - Supports leading FPGA vendor-generated cores
 - FPGA vendor-independent synthesis technology integrates with vendor P&R tools for excellent QoR
 - New Modular Design Flow enables efficient reuse of physically implemented components, thus leveraging previous success in future FPGA designs
- **Improve Designs Quickly**
 - New Placement Reuse Flow speeds time to market by solving performance issues due to last-minute ECOs or changes in functional requirements
 - *PreciseTime* allows "what-if" and incremental timing analysis
 - Automated physical synthesis improves performance and reduces the runtime of subsequent P&R iterations
- **Meet Project Requirements**
 - New Divide and Conquer Flow saves time by targeting optimization to the design portions that need it most
 - *PreciseView*, the placement and timing debug editor, reduces costs and increases performance
 - Cross-probing between RTL, schematic, timing, and physical views of the design enhances analysis

- **Project Management**

- + Captures all aspects of the design information in the project file, encapsulating current status of the design, including constraints and variables
- + Multiple implementations can be created
 - Snapshot design state at any point
 - Compare alternative design approaches
 - Restores all settings, as well as design state
 - Revert to design state at the “last save” point
- + Imports Xilinx project information for physical optimizations

- **Modular Design Reuse Flow**

- + Create optimized, reusable circuit building blocks
- + Relative placement in macros makes them relocatable
- + Blocks can be used in multiple designs, or many places in a single design
- + Quickly optimize designs with regular structures – all occurrences can be updated simultaneously

- **Schematic Generation**

- + Instance and net bundling for readability
- + Allows graphical logic traversal
- + Advanced timing debugging: displays critical path as well as links to source code
- + Integrated timing analysis information via tool-tips
- + Annotate timing information to RTL schematic objects

- **Device-Independent Inference Engine**

- + High-level datapath element inferencing
- + RAMs, ROMs and multipliers
- + DSP inferencing for advanced FPGA architectures

- **Advanced Optimization Algorithms**

- + Advanced FSM optimizations
 - Safe FSMs
 - Automatic or manual state encoding
 - Dedicated synchronous RAM blocks
- + Optimization across boundaries
- + Timing-driven LUT mapping
- + RAM read-write collision glue logic
- + Advanced DSP mapping
- + Advanced ROM to RAM mapping

- **Language Neutrality**

- + Any combination of SystemVerilog, VHDL, Verilog or EDIF
- + Automatic ordering of VHDL sources
- + Automatic top-level design detection
- + Full support for Verilog 2001 language constructs
- + Vendor-generated cores (e.g. Xilinx CoreGens and Altera MegaFunctions)

- **ASIC Prototyping**

- + Gated clock conversion through hierarchy
- + Gated clock conversion for latches, shift-registers, RAM, block multipliers and DSP blocks
- + Conversion of DesignWare® (DW01, DW02 and DW RAM) instances

- **Multiple Platform /OS support**

- + Windows NT/2000/XP; Linux RedHat 7.3, 8.0 or Enterprise WS 3.0 (KDE or GNOME); Sun Solaris 8 or 9

Improve Designs Quickly

- **PreciseTime Timing Analysis Engine**

- + Accepts industry-standard SDC format for constraints
- + Also allows constraints in RTL, or added interactively via the GUI
- + Reads Xilinx UCF+EDIF and Altera QSF+EDIF files
- + Writes vendor constraint files (UCF and QSF/Tcl)
- + Advanced constraints such as multicycle_path, false_path and max_delay
- + Determines missing constraints within your design
- + Reports any clock domain crossings
- + Incremental operation provides instant feedback after constraint changes
- + Interactive, highly configurable timing reports
- + Slack data displayed as histogram

- **Highly Integrated Design Platform**

- + Unified database allows comprehensive cross-probing
 - From logic design to physical implementation
 - From physical placement to logic design
 - From physical placement to RTL source
 - From FPGA vendor timing report to a path schematic or physical placement
- + Integrated FPGA vendor place-and-route flow support
 - Actel Designer 7.2
 - Altera Quartus II 6.0 SP1
 - Atmel ProChip 4.0 Fitter 1.8.8.9, System Designer 3.0 SP3
 - Lattice ispLEVER 6.0
 - QuickLogic QuickWorks 9.8.1
 - Xilinx ISE 8.2
- + Timing analysis data available in every view

- **Physically Aware Analysis**

- + Annotate accurate post-route interconnect delays
 - + Annotated analysis results available in RTL and technology views
 - + Optimization with annotated delays
 - + Tracing capabilities to and from register
-

- **Automatic Physical Synthesis**

- + One-button operation
- + Optimize specific blocks, timing paths, or entire design
- + Advanced physical optimization algorithms
 - Placement optimization
 - Timing-driven re-placement of cells in critical paths
 - Placement-influenced delay estimation for quick convergence
 - Logic retiming
 - Forward and backward retiming
 - Pipelining
 - Logic restructuring to allow retiming
 - Retiming of DSP pipeline registers
 - Register replication
 - Timing-driven selection of replication candidates
 - Timing-driven placement of replicated registers
 - Physical re-synthesis
 - Localized logic restructuring with re-placement
 - Path compression rewires circuit for optimal timing
- + Design is fully placed after physical optimization
 - Improves predictability of optimization results
 - Speeds vendor place-and-route flow

- **Placement Reuse (ECO) Flow**

- + Allows both push-button and interactive ECO flows
- + Save current design placement and re-apply after RTL modifications
- + Unmodified portions of design retain existing placement
- + Timing-driven placement of modified circuitry
- + Algorithm allows nudging of existing placements

Meet Project Requirements

- **TCL-based Command Line Interface**

- + Interactive command environment
- + All operations can be scripted and replayed
- + Full TCL support to allow user program creation
- + Comprehensive design structure and timing data procedural interface

- **PreciseView Layout Editor**

- + Detailed device-specific FPGA fabric display
 - Slices/Lcells with detailed content
 - RAM/ROM/MULT/DSP resource stripes
 - Clock buffers and clock managers (PLLs, DLLs)
 - I/O buffers with internal registers

- + Graphical timing information
 - Color-code instances based on slack
 - Color code routing fly-lines based on slack or fanout
 - Slack graph shows only critical fly-lines
 - Display up to 10 timing paths in physical view
 - Together, these ease the ability to make predictable manual layout changes
 - + Multiple design browsers
 - Hierarchical design view
 - Unplaced cell list
 - Relatively placed macro (RPM) groupings
 - Regions definitions and groupings
 - + Edit layouts manually
 - Move a cell or group of cells
 - Swap cells between two locations
 - Improve placement of a group of cells (timing driven)
 - Interactively replicate individual registers
 - Interactively retime individual registers (forward or backward)
 - Convert specified block RAMs to distributed RAMs
 - Convert specified block ROMs to logic
 - Interactively perform path compression on specified logic
 - Automatic removal of cell overlaps (timing driven)
 - Correct by construction editing
 - Packing rules are enforced
 - Clock regions are honored
 - Macro groupings are maintained
 - Multi-level undo capability for all editing operations
 - + Region management
 - Create/edit region boundaries within the device fabric
 - Assign logic to regions
 - Area place cells within a region (timing driven)
 - Pass region requirements to vendor place-and-route
 - Honors region and group assignment in design source
 - + Relatively placed macros (RPMs)
 - Convert placed cells into relatively placed macros
 - Macros move as a single object in PreciseView
 - Passes RPM information to vendor place-and-route
 - RLOC for Xilinx
 - LOGICLOCK for Altera
 - Honors relative placement needs in design source
 - Automatic unification of RPM groupings
-

- + Detailed view
 - Timing detail at each pin of cell
 - Fly-lines to connected cells indicate direction and timing slack
 - Displays cell instance names and cell site names
 - Window can be undocked for easy access
- + Context view indicates editing location within the device
- + Advanced selection algorithms allow cells to be grouped based on:
 - Area
 - Hierarchy
 - Inclusion within a timing path
 - Included within the critical cover of a cell
 - Inclusion within a macro (e.g. contained within a carry chain)
 - Resource packing (contained within a slice or LCell)

• **Divide and Conquer Flow**

- + Isolates blocks for timing closure iteration
- + All tools, including place-and-route can be used on the block
- + Locks down the rest of the design to avoid creating new issues
- + Greatly reduces design iteration time

• **MacroBuilder Tool Suite**

- + Captures design modules with full netlist and placement information
- + Wraps isolated macro with logic
 - Allows standalone place-and-route of isolated modules
 - Allows standalone physical optimization
- + Creates a relocatable, relatively placed design unit for reuse
- + Interactively overlays circuit module with macro information

FPGA Device Support			
Vendor	Device	Precision RTL	Precision Physical
Actel	3200DX, 40MX, 42MX, 54SX, 54SXA	✓	
	ACT1, ACT2 / 1200XL, ACT3	✓	
	eX, A500K	✓	
	RT54SX/SX-S, Axcelerator	✓	
	ProASIC ^{PLUS} , ProASIC3/3E	✓	
	RTAX-S (includes 4000)	✓	
Altera	MAX II, 3000A, 7000/AE/B/E/S 9000	✓	
	FLEX 6K, 8K, 10K / KA / KB / KE	✓	
	ACEX 1K	✓	
	APEX II, 20K / KC / KE	✓	
	Excalibur-ARM	✓	
	Cyclone	✓	✓
	Cyclone II	✓	
	Excalibur-ARM	✓	
	Mercury	✓	
	Stratix	✓	✓
	Stratix GX	✓	✓
Stratix II	✓		
Stratix II GX	✓		
Atmel	AT40K	✓	
	AT6K02	✓	
	AT6K04	✓	
	AT94K	✓	
	ATF15xx AS / ASV / BE	✓	
Lattice	MACH 4 / 4LV / 4A / 5 / 5LV	✓	
	ispGDx / GDx2 / GDx2-E	✓	
	IspLSI 1K / 2K / 5K / 8K	✓	
	ispMACH 4A / 5000B / 5000VG	✓	
	ispXPLD 5000MX / XPGA / XPGA-E	✓	
	ORCA Series 2CA / 2TA / 3C / 3T / 4E	✓	
	MachXO	✓	
	MachXO 1k/2k	✓	
	EC / ECP-DSP / ECP2-DSP / ECP2M	✓	
	SC / SCM	✓	
QuickLogic	Eclipse	✓	
	Eclipse II / E / Plus	✓	
	QuickMIPS	✓	
	QuickPCI	✓	
	QuickPCI-II	✓	
	QuickRAM	✓	
	pASIC3	✓	
	PolarPro	✓	
Xilinx	XC9500 / XL / XV	✓	
	Automotive families	✓	
	CoolRunner families	✓	
	Spartan2	✓	
	Spartan2E	✓	✓
	Spartan3 / A / E	✓	
	Spartan3L	✓	✓
	Virtex	✓	
	Virtex-E	✓	✓
	Virtex-2, Virtex-2 Pro	✓	✓
	Virtex-4	✓	✓
	Virtex-5	✓	
	QPro Virtex-E Military	✓	✓
	QPro Virtex-II Military	✓	✓
	QPro Virtex-II Rad Tolerant	✓	✓
	QPro Virtex Hi-Rel	✓	
QPro Virtex Rad-Hard	✓		

To learn how Precision Synthesis can address your FPGA design needs, call Mentor Graphics to schedule a product demonstration, or visit our website for the latest product news and information at www.mentor.com/synthesis

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Corporate Headquarters
Mentor Graphics Corporation
8005 SW Boeckman Road
Wilsonville, OR 97070-7777
Phone: 503-685-7000

Sales and Product Information
Phone: 800-547-3000
503-685-8000

Silicon Valley Headquarters
Mentor Graphics Corporation
1001 Ridder Park Drive
San Jose, CA 95131 USA
Phone: 408-436-1500
Fax: 408-436-1501

North American Support Center
Phone: 800-547-4303

Europe Headquarters
Mentor Graphics Corporation
Immeuble le Pasteur
13/15, rue Jeanne Braconnier
92360 Meudon La Forêt
France
Phone: 33 (0) 1-40-94-74-74
Fax: 33 (0) 1-46-01-91-73

Pacific Rim Headquarters
Mentor Graphics (Taiwan)
Room 1603, 16F
International Trade Building
No. 333, Section 1, Keelung Road
Taipei, Taiwan, ROC
Phone: 886-2-87252000
Fax: 886-2-27576027

Japan Headquarters
Mentor Graphics Japan Co., Ltd.
Gotenyama Hills
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140
Japan
Phone: 81-3-5488-3030
Fax: 81-3-5488-3021



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