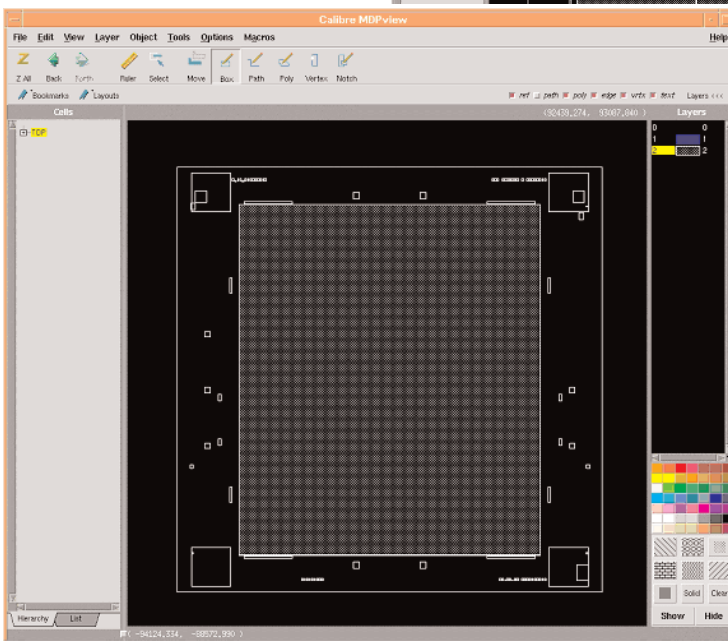
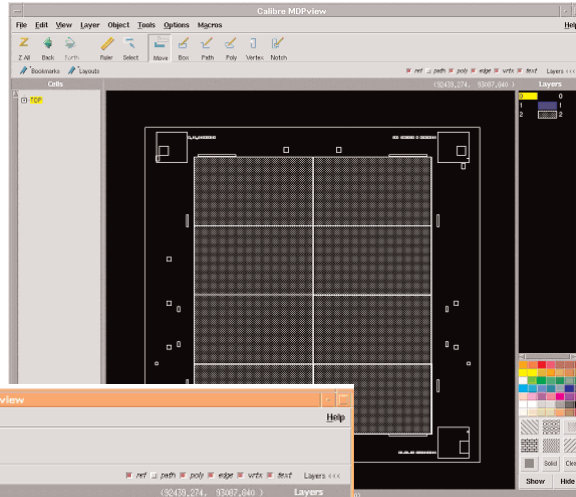


*Calibre MDPmerge, part of Calibre's MDP tool suite from Mentor Graphics, enables the merge of chip placements in VSB11 jobdecks as the precursor to mask writing.*



*The illustration shows a VSB11 jobdeck before (above) and after (left) the merge operation has been conducted.*

## Key Product Benefits

- Merges individual chips for mask writing tolerance and throughput optimization
- Completes the data preparation flow for VSB11 format
- Easy parameterized tuning for various mask writer types
- Dynamic memory allocation
- 32- and 64-bit in HP, Sun and Linux platforms
- Multi-threading and distributed processing with excellent scaling performance
- Integrated with Calibre design-to-silicon platform

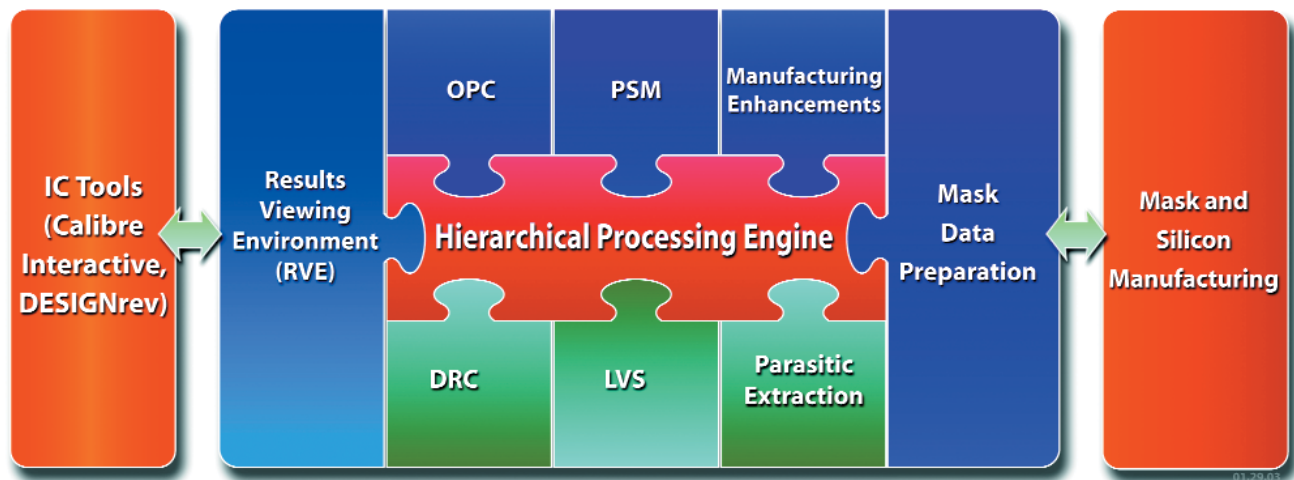
## Calibre MDPmerge - Merging chips in VSB11 jobdecks

Calibre® MDPmerge extends the Calibre's mask data preparation (MDP) product line, which includes data preparation utilities to generate, view and verify mask data. As part of Calibre's design-to-silicon platform, it enables a continuous flow from physical verification (DRC/LVS) and resolution enhancement techniques (RET) to the completion of mask data preparation.

The generation of the individual pattern files in VSB11 format using the Calibre FRACTUREt tool results in chip data sets optimized for fastest mask writing and tight CD control. The subsequent assembly of the individual chips through a jobdeck can be further optimized by streamlining the writing sequence as well as by enabling accurate correction of proximity effects. This is accomplished by merging individual chip placements into a single chip along with the update of the placement information. MDPmerge offers this functionality by deploying Calibre's powerful hierarchical engine along with parallel processing methods in SMP and distributed computer environments. This enables fast processing speeds in addition to an optimization of the output for most efficient mask writing.

## Calibre MDP Tools and Capabilities

- Calibre FRACTUREm
- Calibre FRACTUREj
- Calibre FRACTUREt
- Calibre MDPverify
- Calibre MDPview
- Mask rule checking
- Mask process correction



The Calibre tool suite offers a complete design-to-silicon solution to ensure a confident design for manufacturing.

## Calibre Offers a Complete Design-to-Silicon Solution

A powerful hierarchical engine is at the heart of the Calibre tool suite, which offers a complete IC and SoC design-to-manufacturing solution. Each tool is an excellent point tool on its own, but the combination of Calibre DRC, Calibre LVS and Calibre RVE (results viewing environment) with Calibre xRC, Calibre RET and Calibre MDP, simplifies and strengthens the design flow.

Calibre xRC parasitic extraction tool accurately models the parasitic effects of passive interconnects that can cause design failure in deep submicron IC designs. Automated interfacing of Calibre LVS to Calibre xRC provides simplicity (one rule file, one invocation) and automated back annotation for accurate parasitic extraction results, and ensures accurate and intentional device extraction with parameter calculation and parasitic device extraction for accurate simulation.

Calibre Interactive™ complements the Calibre physical verification tool suite by enabling designers to perform verification from within Cadence® Virtuoso and Mentor Graphics IC Station and Calibre DESIGNrev. Together with Calibre RVE, Calibre Interactive provides a seamless, push-button interface, enabling designers to use a single platform for cell/block and full-chip physical verification.

The Calibre RET tool suite for Optical and Process Correction (OPC), Phase Shift Mask (PSM), Scatter Bars (SB) and Off-Axis Illumination (OAI) deliver silicon accuracy, fastest turn-around-time and excellent yield.

Calibre MDP allows for seamless continuation of the data manipulations required for RET techniques to the mask data format conversion in one batch run, keeping data hierarchically represented as long as possible.

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