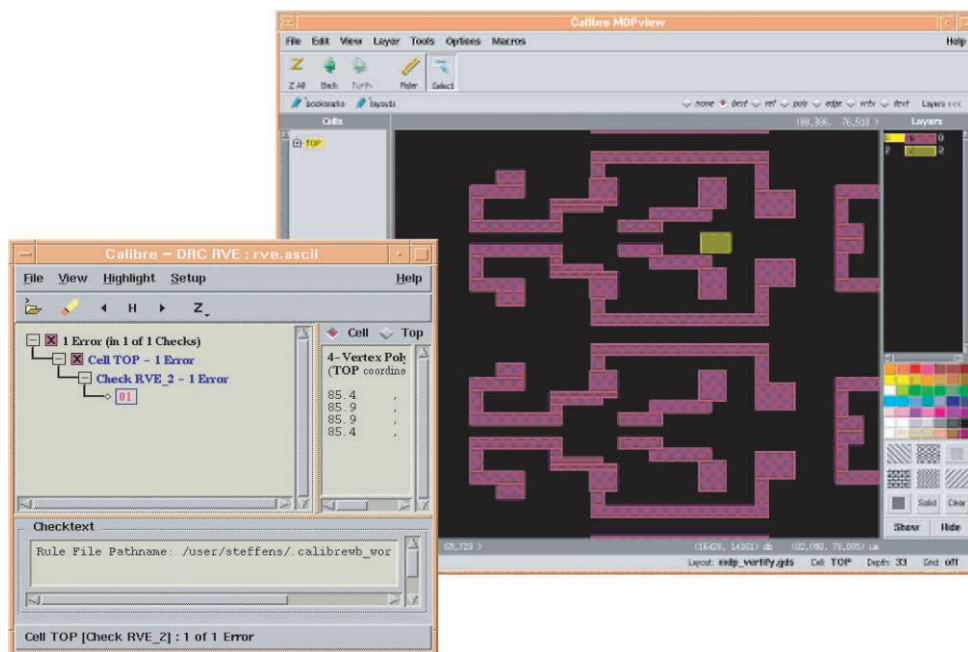


Calibre MDPverify Mask Data Verification Comparison

Manufacturability

D A T A S H E E T



Calibre MDPverify is the verification of mask writer formatted data by comparison against another file or the original GDS-layer. It is part of Calibre's MDP tool suite offered by Mentor Graphics. The illustration shows a difference detected during the comparison run and highlighted using Calibre RVE, the result viewing environment.

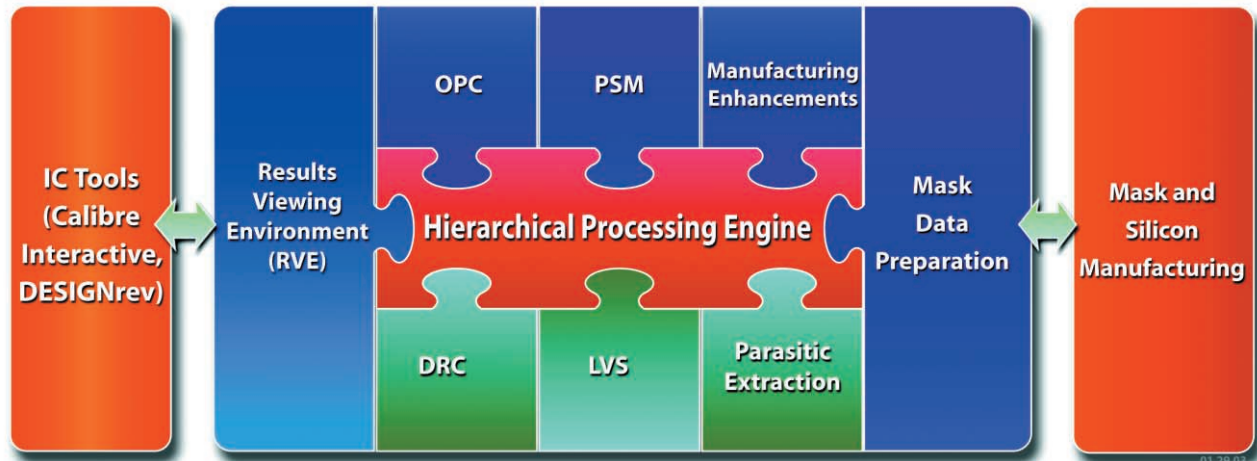
Calibre MDPverify: Mask Data Verification for Comparison of Original Data and Version Control

Calibre MDPverify™ builds on Calibre's core competency in the design verification area. It enables the verification of the final mask writer data against its original GDS-layer, thus preventing mask writing with erroneous data. It supports the tracking of design updates by confirming the presence of desired changes in the final mask data. The comparison is not connected to a fracture step and thus independent. Calibre MDPverify compares flexibly all available output formats against GDS, e.g. MEBES to GDS, against itself, e.g. JEOL to JEOL, but also across the formats, e.g. JEOL-MEBES.

In addition to multi-threaded computing, special file handling techniques allow for fast processing of the comparison step. The results can be automatically classified and assessed, and are efficiently visualized with Calibre's result viewing environment (RVE).

Key Product Benefits:

- Build on hierarchical geometry processing inside the Calibre database
- 32/64 bit on HP, Sun and Linux platforms
- Multi-threading with significant scaling performance
- Matching of files with different scale and transformations
- Verification of mask writer data against the original GDS layer
- Version control for subsequent releases
- Cross format comparison - e.g., JEOL-MEBES
- Dynamic memory allocation
- Easy to integrate in an OPC and verification flow
- Flexible result classification with SVRF based scripts



The Calibre tool suite offers a complete layout to silicon solution to ensure a confident design for manufacturing.

Complete Design-to-Silicon Solution

A powerful hierarchical engine is at the heart of the Calibre tool suite, which offers a complete IC and SoC design-to-manufacturing solution. Each tool is an excellent point tool on its own, but the combination of Calibre DRC, LVS and RVE with xCalibre, Calibre xRC, Calibre RET and Calibre MDP simplifies and strengthens the design flow.

xCalibre, for analog/flat designs and libraries, and Calibre xRC, for large, hierarchical designs, accurately model the parasitic effects of passive interconnects that can cause design failure in deep submicron IC designs. Automated interfacing of Calibre LVS to xCalibre/Calibre xRC provides simplicity (one rule file, one invocation), automated back annotation for accurate parasitic extraction results, and ensures accurate and intentional device extraction with parameter calculation and parasitic device extraction for accurate simulation.

Calibre Interactive complements the Calibre physical verification tool suite by enabling designers to perform interactive invocation from within Cadence's Virtuoso and Mentor Graphics' IC Station and Calibre DESIGNrev. Together with Calibre RVE (Results Viewing Environment), Calibre Interactive provides a seamless interface within many design environments, enabling designers to use a single platform for interactive cell/block and full-chip physical verification.

The Calibre RET tool suite for Optical and Process Correction (OPC), Phase Shift Mask (PSM), Scatter Bars (SB) and Off-Axis Illumination (OAI) deliver silicon accuracy, fastest turn-around-time and excellent yield.

Calibre MDP allows for seamless continuation of the data manipulations required for RET techniques to the mask data format conversion in one batch run, keeping data hierarchically represented as long as possible.

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