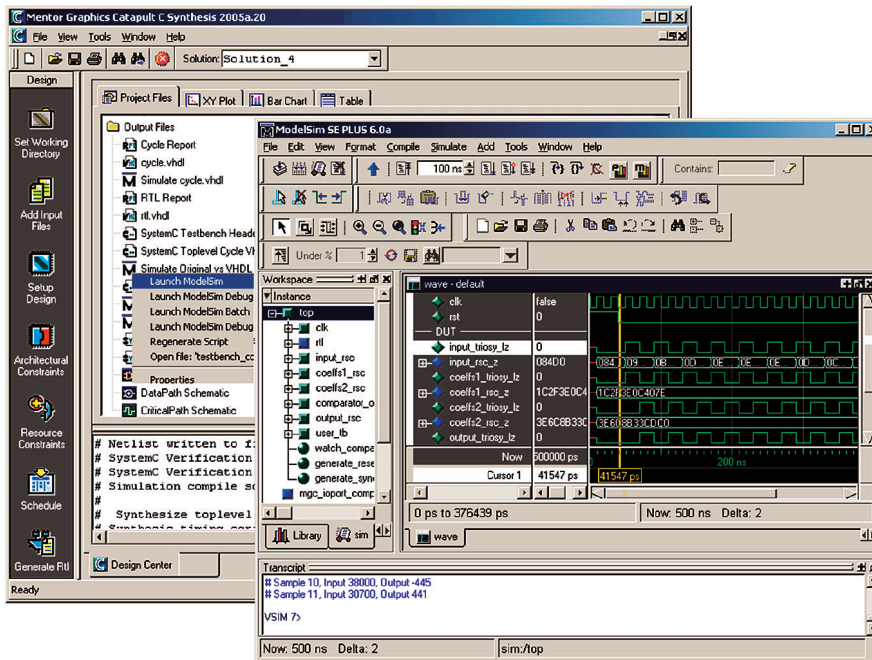


Catapult C Synthesis

Automated Verification Extension

C-Based Design

D A T A S H E E T



Major product features:

- Push-button RTL verification
- Accelerated system verification
- ANSI C++ testbench reuse
- Push-button ModelSim integration
- Automatic SystemC Transactor Generation
- Automated SystemC Wrapper Generation
- Automatic SystemC RTL, Cycle and untimed TLM (2H'05) for faster system level verification
- Multiple output languages include Verilog, VHDL and SystemC
- OSCI compliant SystemC output

Catapult C Synthesis's automated verification allows the user to verify the original C source against the generated RTL netlist in a push-button fashion.

Bridging the ESL Gap Between Synthesis and Verification

Each move from one abstraction layer to another typically increases simulation performance by an order of magnitude. As ASICs become ever more complex with millions of gates, designing at a higher level of abstraction using languages like pure ANSI C++ provides substantial productivity gains over traditional RTL design methodologies.

Unfortunately, the huge productivity gains achieved by adopting algorithmic synthesis can quickly be negated by traditional iterative verification techniques. To boost overall system level verification, designers often use mixed abstraction models such as SystemC™ transaction level models combined with RTL models. However, developing these higher abstraction models involves the time-consuming process of inserting hardware like details such as hierarchy, concurrency, and interface protocol. This manual process, called progressive refinement, requires the designer to develop and maintain multiple abstraction models as well as the hardware testbench and transactors for various design interfaces.

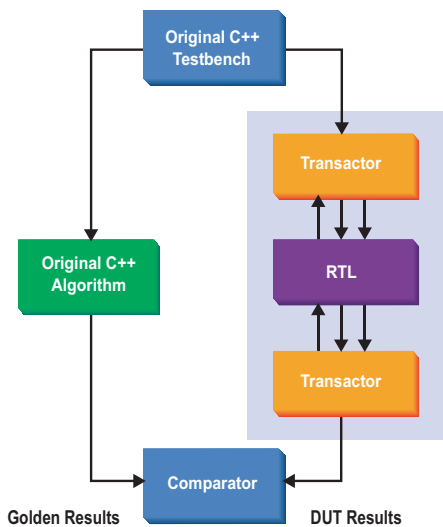
Catapult C Synthesis Verification Extension

The new automated verification extension for Catapult™ C Synthesis directly addresses this bottleneck by combining algorithmic C synthesis with automated verification to efficiently bridge the gap between design creation and verification in an ESL design flow. The environment not only automates ANSI C++ to RTL, but also automates ANSI C++ to verification providing both C++ testbench reuse for the RTL designer as well as multi-abstraction model generation for the system designer. Catapult C Synthesis automatically generates interfaces to the design, allowing the user to perform detailed design architecture analysis and optimization without having to progressively refine the verification testbench, models and transactors.

Catapult C Synthesis enables mixed abstraction verification by automatically generating both RTL and behavioral SystemC models. The behavioral SystemC models generated are both cycle- and pin-accurate while optimized to simulate 10 - 20 times faster than RTL. The integrated verification flow provides push-button simulation with OSCI-compliant simulators such as ModelSim® from Mentor Graphics.

	Source	Simulation	Implementation
Function arguments → ANSI C++	Functional	10,000x (1 minute)	20x (2 days!!)
Transaction → Untimed TLM SystemC	Structural	1,000x	
Transaction → Timed TLM SystemC	Transaction	100x	
Protocol → CycleAccurate TLM SystemC	Cycle	10x	2x (2 weeks)
Protocol → RTL SystemC	RTL	1x (7 days)	1x (5 weeks)

Productivity gain due to moving from one layer of abstraction to another.



Catapult C Synthesis automatically creates the SystemC Transaction Level wrappers that enable reuse of the original C test bench.

Abstraction Drives the Benefit

The automated verification flow in Catapult C Synthesis extends productivity gains achieved during the synthesis process to verification by allowing designers to mix abstraction levels during the verification process. A design can be described and verified using various levels of abstraction ranging from traditional pin-accurate timed RTL to pure ANSI C++ algorithmic descriptions. The benefit is at higher levels of abstraction, where designs can be functionally validated up to 10,000 – 100,000 times faster than RTL verification.

Rapid RTL Verification Through Test Bench Reuse

Catapult C Synthesis enables designers to reuse their existing high speed, ANSI C++ testbench for verifying Catapult's RTL Verilog or VHDL output. Catapult C automates this process by generating the necessary SystemC wrappers and transactors that allow the RTL output to co-simulate with the original ANSI C++ test bench to provide push-button functional verification. The same framework can easily extend to hardware emulation and prototyping.

Accelerated System Verification

In a mixed abstraction level simulation environment, transactors are used to connect blocks modeled at different abstraction levels in a system. However, in a traditional Transaction Level Modeling (TLM) based verification environment, the transactors are created manually — a long error-prone process that is often as complex and time consuming as the creation of the RTL model itself. Moreover, new transactors must be created as the design interface changes, leading to many manual iterations. The Catapult C Synthesis Verification Extension automatically generates the SystemC transactors, enabling its cycle accurate RTL output to co-simulate with higher abstraction level models. The flow has the added benefit of being able to plug into any TLM-based verification environment.

Visit our web site at www.mentor.com/c-based_design for more information.

Copyright © 2005 Mentor Graphics Corporation.
SystemC and Catapult are trademarks and ModelSim and Mentor Graphics are registered trademarks of Mentor Graphics Corporation.
All other trademarks mentioned in this document are trademarks of their respective owners.

Corporate Headquarters
Mentor Graphics Corporation
8005 S.W. Boeckman Road
Wilsonville, Oregon 97070 USA
Phone: 503-685-7000
North American Support Center
Phone: 800-547-4303
Fax: 800-684-1795

Silicon Valley
Mentor Graphics Corporation
1001 Ridder Park Drive
San Jose, California 95131 USA
Phone: 408-436-1500
Fax: 408-436-1501

Europe
Mentor Graphics
Deutschland GmbH
Arnulfstrasse 201
80634 Munich
Germany
Phone: +49.89.57096.0
Fax: +49.89.57096.400

Pacific Rim
Mentor Graphics Taiwan
Room 1603, 16F,
International Trade Building
No. 333, Section 1, Keelung Road
Taipei, Taiwan, ROC
Phone: 886-2-27576020
Fax: 886-2-27576027

Japan
Mentor Graphics Japan Co., Ltd.
Gotenyama Hills
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140
Japan
Phone: 81-3-5488-3030
Fax: 81-3-5488-3031

Mentor Graphics



Printed on Recycled Paper

6-05 C&A

1023860