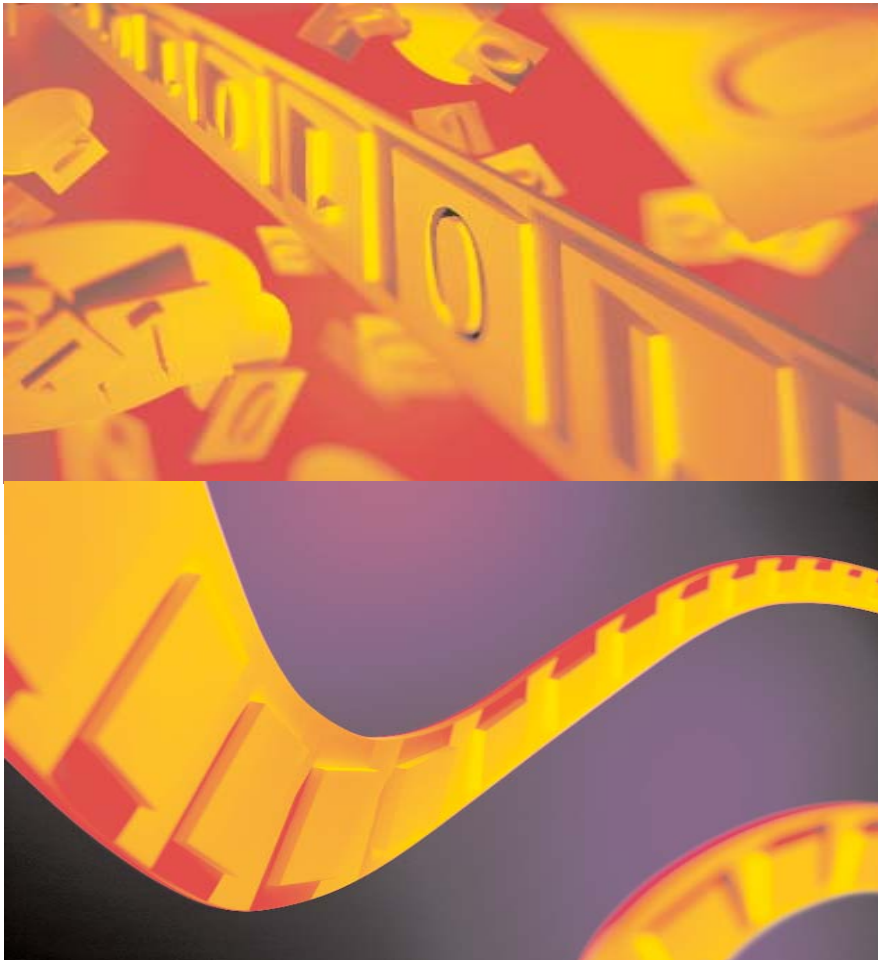


DFTADVISOR & FLEXTTEST

TEST SYNTHESIS, SEQUENTIAL ATPG & MORE

Design-for-Test

D A T A S H E E T



DFTAdvisor and FlexTest offer comprehensive solutions for test synthesis and sequential ATPG.

INSERTING TEST STRUCTURES

Design-for-testability includes the insertion of test structures such as scan, test points, and/or other types of test logic. DFTAdvisor™ is a test synthesis tool that provides all of this and more.

DFTAdvisor is a powerful and flexible tool for inserting and verifying complex scan and test point logic.

FAULT SIMULATION & SEQUENTIAL ATPG

For designs with few or no inserted test structures, functional test and/or sequential ATPG are the only options. FlexTest™ fault grades a design's functional vectors. The tool's sequential ATPG capabilities can then target the undetected faults for test coverage improvement. When teamed with FastScan™, FlexTest can offer top-up ATPG coverage on a design's non-scan circuitry.

DFTADVISOR FEATURES

- Provides intelligent scan insertion and connection at all levels of design hierarchy
- Supports Mux-DFF, Clocked-Scan, LSSD, and mixed design styles
- Inserts full scan and offers several different methods of partial scan selection
- Performs extensive design rules checking to identify testability trouble spots early in the design cycle
- Automatically corrects many common testability problems
- Supports layout-based scan ordering for optimal chain layout
- Inserts IEEE 1500 compliant test structures to enable block-based testing strategies for SoC designs

FLEXTTEST FEATURES

- Fault simulates functional vectors
- Performs ATPG for non-scan and partial scan designs
- Supports stuck-at, IDDQ and transition fault models
- Works with FastScan to top-up test coverage for sequential circuitry
- Shares common libraries and fault lists with FastScan
- Shares common commands and has same user interface as FastScan to ensure an easy path to a structured test approach



OTHER SOLUTIONS IN THE ATPG PRODUCT FAMILY

Graphical Debug

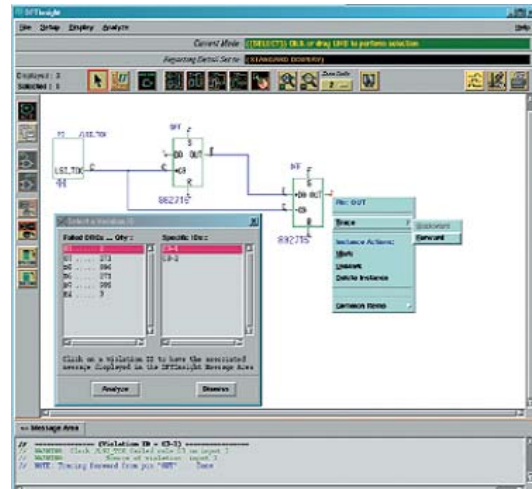
Troubleshooting testability problems can be a difficult process – unless it's automated in a graphical environment like DFTInsight™. The graphical debugging environment simplifies analysis of testability problems. The tool generates a schematic view to display information, making it easier to isolate and correct testability problems.

DFTInsight Features:

- Offers graphical analysis of testability rule violations to reduce testability debug time
- Displays pertinent schematic and simulation data to isolate and identify testability problems
- Displays a variety of user-selectable data and allows interactive design traversing for flexible design analysis
- Integrates with and supported by the Mentor Graphics FastScan, TestKompress®, FlexTest™, DFTAdvisor™, and LBISTArchitect™ DFT tools

Design Complexity, SoCs, and Whole Chip Testing

The diverse design structures integrated onto a typical SoC design require various methods to ensure comprehensive testing. While high-quality, compact tests for a design's logic is important, it's just one part of a whole-chip test methodology.



DFTInsight provides an easy-to-use graphical troubleshooting environment that accelerates test debug and generation of high-coverage test sets.

DFTAdvisor and FlexTest are part of the Mentor Graphics technology-leading DFT tool suite, which includes integrated solutions for scan, ATPG, Test time/data compression, advanced memory test, logic BIST, boundary scan, diagnosis, and a variety of DFT-related flows. All Mentor DFT tools are available on UNIX and Linux platforms. For more information, visit www.mentor.com/dft.

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03/2006 1024520-w
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