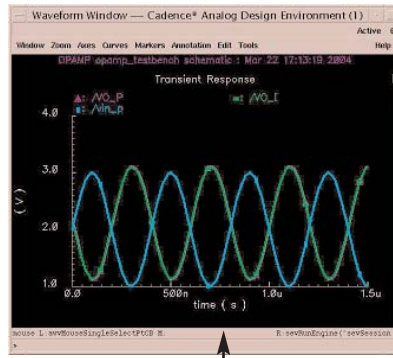
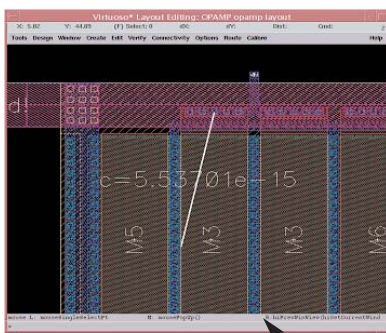


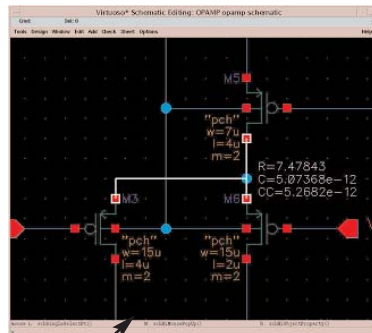
Simulation setup



Plot waveforms



Cross-probe



Key Product Benefits:

- **Seamless Invocation, Integration and Cross-Probing.** Calibre xRC is easily invoked using Calibre Interactive. Designers can cross-probe results between layout, schematic, source netlist, layout netlist and LVS results. Results are accessed by Calibre View and Calibre RVE, both integrated into popular design frameworks.

Hierarchical netlisting capabilities.

When paired with a post layout hierarchical simulation tool, such as HSIM, Calibre xRC provides a manageable hierarchical netlist for large designs.

Full-Chip, Transistor-Level Parasitic Extraction. Calibre xRC capability is derived from the Calibre hierarchical engine for excellent performance and accuracy on memory, analog, SoC and ASIC designs.

Tight Integration with Calibre LVS, the industry standard for physical verification. By reading LVS data structures directly, Calibre xRC provides complete circuit netlist information integrated to the source schematic for back-annotation.

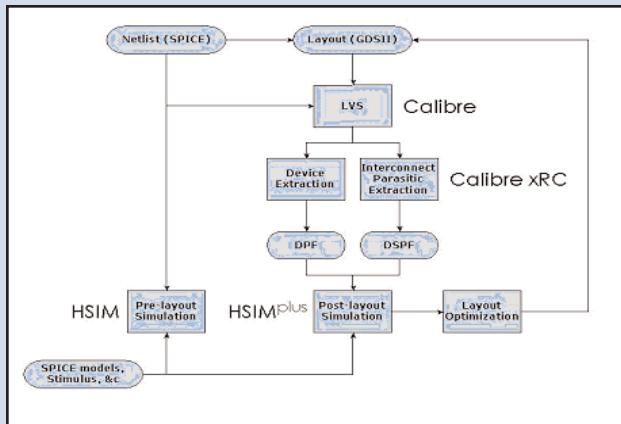
- **Mixed-Level Output for Downstream Analysis.** All transistor- and gate-level parasitic data (C, RC, RCC) is stored and on-call in the Calibre xRC parasitic database to enable multiple analysis flows.

- **One Rule File, One Flow.** A single parasitic extraction flow streamlines the SoC design flow, reduces cycle time, eliminates multiple-tool maintenance, and ensures a confident data transfer.

Challenges of the Nanometer Era: Accurate Silicon Modeling and Hierarchical Netlisting Capabilities

The nanometer era has revealed significant concerns: physical effects are now the leading factor in the failure to achieve acceptable yield. However, current silicon-modeling techniques are unable to accurately predict if designs will successfully manufacture. Traditional methods of black boxing, assumptive device measurement and gate-level extraction are not sufficient to meet the accuracy requirements of simulating sophisticated IC designs. This is a task that can only be accomplished through exacting detail-actual device measurement and transistor-level parasitic extraction-evaluated across the characteristics of the entire design.

Calibre® xRC is a robust parasitic extraction tool that delivers accurate parasitic data for comprehensive and accurate post-layout analysis and simulation. Calibre xRC is able to extract interconnect parasitics hierarchically. The result is a compact, hierarchical, transistor-level parasitic data, which can be back-annotated and simulated with full-chip circuit simulation tools, such as HSIM. By using hierarchical storage and leveraging the circuit hierarchy and isomorphism during simulation, Calibre xRC and HSIM achieve breakthrough performance for very large circuits, while delivering detailed SPICE-level accuracy.



Hierarchical DSPF back-annotation flow with Calibre xRC and HSIM.

Calibre xRC and HSIM: Managing the Hierarchical, Transistor-level Post-layout Analysis Flow

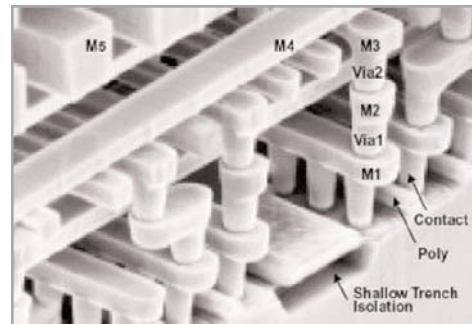
As process sizes continue to shrink, integrated circuit designers are forced to address an increasing number of analysis issues that impact design closure, such as timing, power, cross-talk noise and signal integrity. For some types of designs, such as memories, these analysis methods require the simulation of full-chip, transistor-level parasitic effects. One of the biggest challenges designers face is the vast amount of parasitic data generated in the process with the resulting bottleneck—the simulation of these large netlists. A combination of high-performance tools provides an efficient solution that minimizes parasitic netlist size while delivering the necessary extraction accuracy; coupled with fast, SPICE-level accurate, hierarchical simulation performance. Designs with a very regular design structure and high hcell reuse, such as memories, will benefit the most from hierarchical parasitic extraction and analysis.

Calibre xRC is able to extract interconnect parasitics hierarchically. The result is a compact, hierarchical, transistor-level parasitic data, which can be back-annotated and simulated with full-chip circuit simulation tools, such as HSIM. By using hierarchical storage and leveraging the circuit hierarchy and isomorphism during simulation, HSIM achieves breakthrough performance for very large circuits, while delivering detailed SPICE-level accuracy.

Accuracy in Device Modeling: Critical Link of Calibre LVS & Calibre xRC

In order to accurately model and analyze nanometer designs, designers must be able to integrate parasitic information into their design environment, and post-layout information must be integrated as an entire circuit or subcircuit suitable for simulation. This requires accurate extraction of intentional devices, physically measured parameters and the ability to properly back-annotate devices, gates, and nets from the layout with the original design source.

To enable this, a tight integration between the LVS and parasitic extraction tools is required. Proper back-annotation for simulation in any of the multiple transistor level flows requires a connection to an LVS tool that enables multiple parasitic extraction flows. The tools need to provide accurate intentional device recognition for the variety of devices (transistor, inductor, capacitor, varactor, etc.) that will be implemented in today's AMS designs.



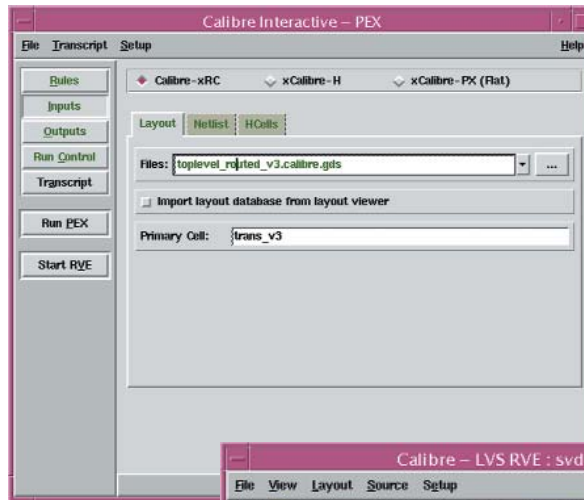
A copper process cross-section reveals complex interactions of metal, poly, interconnect, diffusion and vias, all potential sources of unintentional physical effects. Photo source: TSMC.

In addition, Calibre xRC's new resistance and capacitance engines, combined with Calibre LVS (layout vs. schematic) fully comprehend the boundary of the BSIM4.0 simulation model to accurately measure, extract and analyze these new parasitics in a geometrically accurate way with smaller netlists, helping to preserve performance, capacity and yield.

Tight integration among the design environment, LVS tool, parasitic extraction tool and analysis tool ensures efficient data handling for both upstream design creation environments and downstream post-layout analysis. When a hierarchical-based LVS tool is paired with a transistor-level parasitic extraction tool, it offers the designer the analysis capabilities required of an AMS SoC design: intentional device recognition (with exact device parameters); parasitic device extraction at both transistor and gate levels; highest accuracy for post-layout simulation; and backannotation of simulation results to the source schematic.

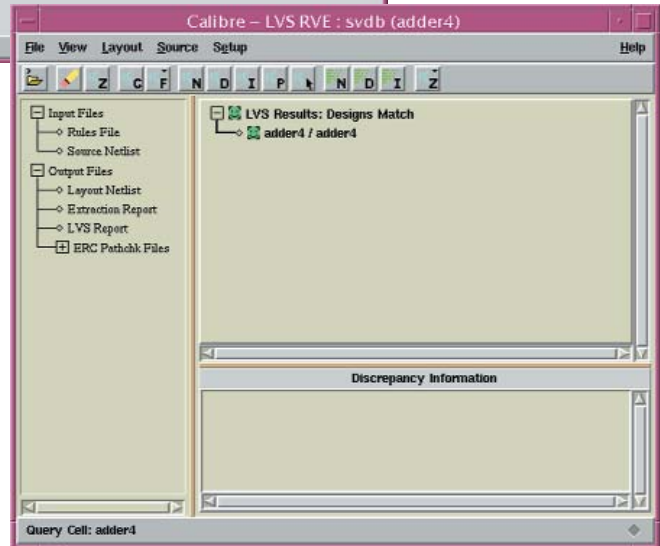
Calibre xRC for Seamless Upstream Integration

- Transistor-Level Integration with Calibre LVS.** For parasitic netlists to be useable in the designer's simulation testbench, the extracted layout netlist, including parasitic devices, needs to be back-annotated to the schematic netlist. A seamless interface between LVS and extraction is critical. When Calibre xRC is used with Calibre LVS, it offers intentional device recognition (with device parameters) and parasitic device extraction at both the transistor and gate levels to provide the highest accuracy for post-layout simulation and to enable back-annotation of simulation results to the source schematic.
- Integrated with various design flows.** Calibre xRC is fully integrated with analog, memory and mixed signal flows for today's SoC designs.
- Integrated with Place and Route flows.** Calibre xRC reads LEF/DEF and annotated GDS data produced by place and route tools, taking advantage of the connectivity information to produce gate-level netlists for gate-level simulators. With the LVS/extraction flow, Calibre xRC supports DEF with GDS and gate-level extraction on full GDS data to provide transistor-level information or to enhance the accuracy of gate-level results with parasitic information from the cells.
- Calibre xRC with Calibre Interactive.** Calibre xRC is fully integrated with Calibre Interactive, giving users access to interactive extraction from within popular layout environments, such as Mentor Graphics IC Station, Cadence® Virtuoso and the Synopsys® Milkway and Galaxy environments.
- Parasitic Browsing with Calibre RVE.** Calibre RVE (results viewing environment) enables viewing of R, C, RCC results in the layout environment.



Calibre is invoked from within the layout environment via the Calibre Interactive graphic user interface.

Calibre's results viewing environment (RVE) displays parasitic results with a tight link to Calibre LVS. From the RVE menu, you can open the parasitic browsing window, shown below.

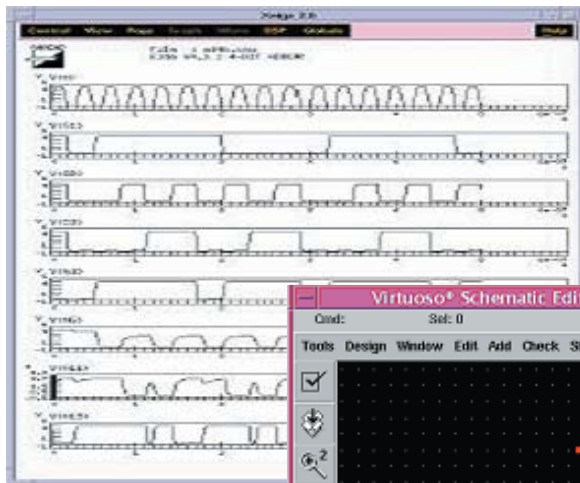


Parasitic Nets in adder4

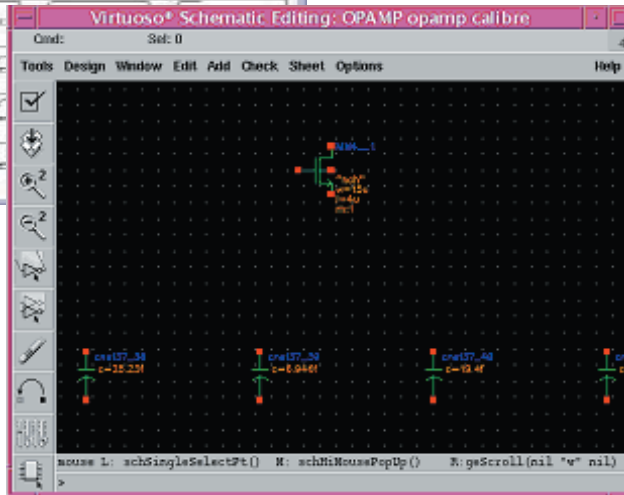
L.Net	S.Net	R (ohm)	C (F)	CC (F)	C+CC (F)
INB3(0)	INB0(3)	334.826	1.80462e-15	6.21754e-16	2.42637e-15
INB3(1)	INB1(3)	217.809	1.4475e-15	8.37268e-16	2.28477e-15
INB0(2)	INB0(2)	334.826	1.80462e-15	6.21754e-16	2.42637e-15
INB1(2)	INB1(2)	217.809	1.4475e-15	8.37268e-16	2.28477e-15
INB0(1)	INB0(1)	334.826	1.80462e-15	6.21754e-16	2.42637e-15
INB1(1)	INB1(1)	217.809	1.4475e-15	8.37268e-16	2.28477e-15
INB0(0)	INB0(0)	334.826	1.84692e-15	5.82733e-16	2.42965e-15
INB1(0)	INB1(0)	217.809	1.59198e-15	6.86541e-16	2.27852e-15
9	net018	413.446	2.7934e-15	2.41376e-15	5.20717e-15
10	net014	413.446	2.79241e-15	2.41773e-15	5.21014e-15
11	net019	413.446	2.7953e-15	2.41402e-15	5.20932e-15
OUT(3)	OUT(3)	69.9884	4.48602e-16	2.97485e-16	7.46088e-16
OUT(2)	OUT(2)	69.9884	4.48602e-16	2.97485e-16	7.46088e-16
OUT(1)	OUT(1)	69.9884	4.48602e-16	2.97485e-16	7.46088e-16
OUT(0)	OUT(0)	69.9884	5.09446e-16	2.21572e-16	7.31018e-16
COUT	COUT	69.5633	3.8195e-16	1.50398e-16	5.32347e-16
X4/8	XI7/net6	166.87	9.89659e-16	1.00996e-15	1.99962e-15
X4/9	XI7/net21	393.867	1.9459e-15	1.37124e-15	3.31714e-15
X4/10	XI7/net18	198.407	6.96146e-16	6.10372e-16	1.30652e-15

Show coupling to: layout net(s)

72 of 72 parasitic nets listed



Simulation results of a full-chip design using Mentor Graphics Mach TA simulation tool.



Calibre View in the Virtuoso environment, showing intentional devices and extracted parameters at top of screen, and parasitic devices and their extracted values at bottom of screen.

Calibre xRC Advanced R and C Engines

Calibre xRC's new **resistance engine** provides improved fracturing, including precise width and resistor location for electro migration analysis. It also offers enabling technologies for inductance extraction and improved device pin handling, improved gate pin placement and user control over gate region extraction. Additionally, the algorithms are hierarchical and much more efficient. Better performance and capacity is attained using the new paradigm while still providing improved accuracy.

Calibre xRC's new **capacitance engine** delivers a much tighter correlation to field solver and silicon data, greatly improving overall accuracy of results. In addition, it has incorporated special models for vias, contacts and the poly-to-contact area, as these are quite susceptible to significant and elusive capacitance effects. Other solutions are taking mathematical shortcuts to modeling that will get them quick extraction results, but will break down later in the design flow. Calibre xRC gives designers greater confidence in their post-layout simulation results, and therefore they do not have to build in prohibitive design margins.

Calibre xL offers parasitic self-inductance extraction integrated with Calibre xRC parasitic RC extraction data, enabling accurate analysis of high frequency effects in nanometer technology. (See the Calibre xL datasheet available at www.mentor.com).

Calibre xRC for Accurate Downstream Analysis

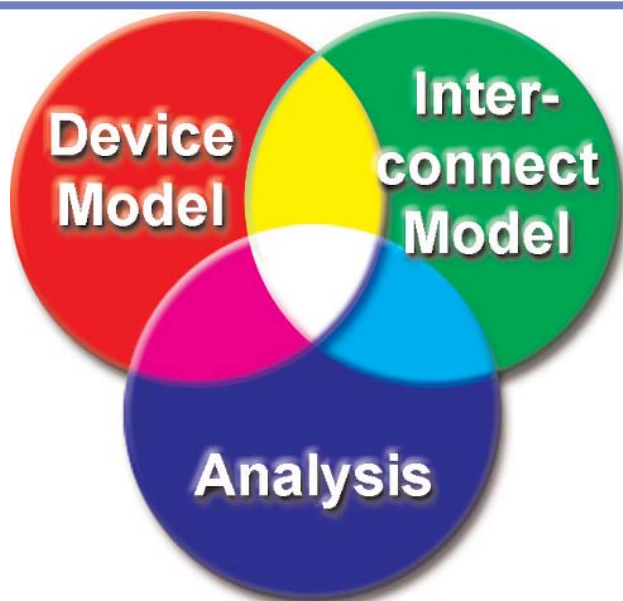
Calibre xRC with Calibre View.

Calibre extracted view provides an automated method for re-simulation directly from the design layout environment. It is supported in the Calibre xRC flow, enabling graphical back-annotation and netlisting.

- **Parasitic Database Provides Variety of Net Models.** Calibre xRC parasitic database provides incremental, hierarchical and multiple electric views to enable analysis flows, including noise, timing, power and signal integrity.
- **Hierarchical netlisting capabilities with HSIM.** Calibre xRC has the ability to output optimized hierarchical parasitic data for signal and power net analysis, integrating with Nassda's post-layout hierarchical simulation tool, HSIM.
- **On-the-Fly Reduction.** The reduction supported in Calibre xRC includes Ticer (combination of AWE and S-parameter techniques) and user-controlled thresholds and tolerances. Calibre xRC reduces parasitic data, thereby reducing netlist size and improving simulation performance, while maintaining accuracy. (Visit www.mentor.com/dsm to download the technical publication titled TICER: Realizable Reduction of Extracted RC Circuits.)
- **Mixed-Level Extraction Enabled by a Parasitic Database.** Calibre offers mixed-level data (transistor, gate and hierarchical) in the same parasitic extraction run with detail for R, C, RCC analysis.
- **Supports industry standard formats** including Spice, DSPF and SPEF outputs for running Mach TA, Eldo, Advance MS, Calibre extracted view and Cadence® Spectre, as well as other standard tools.

Calibre xRC: The Comprehensive Solution for Nanometer Silicon Modeling at 90nm

While nanometer technology enables more and more functionality on a single chip, it also brings a host of new physical effects that must be accounted for in simulation and modeling. Finer line widths, longer interconnect, more routing layers and burgeoning analog content are just the top of the iceberg; lurking below are via capacitance, poly-contact coupling, planarity fill, antenna effects, copper processing issues, parasitic inductance and much more that can produce functional flaws, which many times result in failed silicon and costly respins. By implementing an advanced nanometer silicon modeling flow that includes Calibre xRC, designers can account for the complex device and interconnect issues that so profoundly affect the accuracy of analysis and successful manufacture of a design.

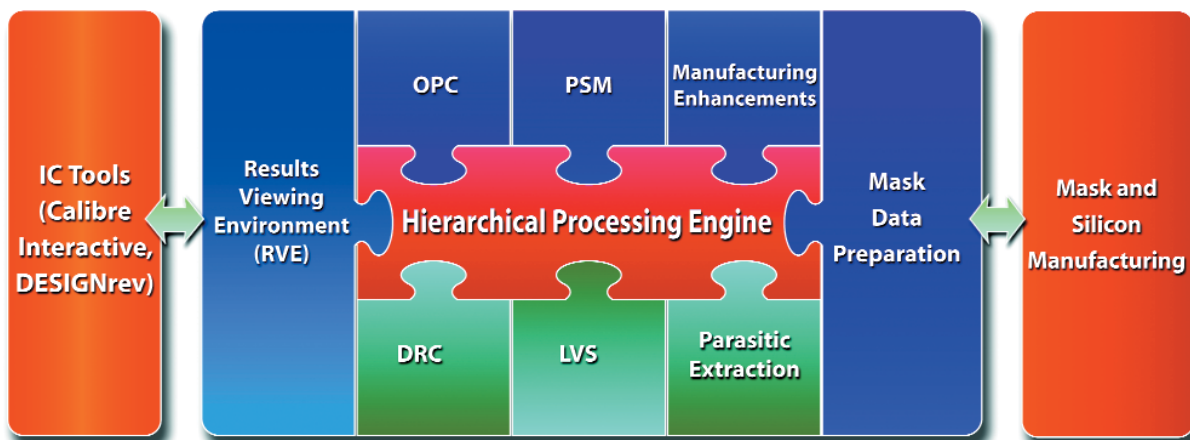


Calibre xRC solves nanometer design issues by capturing complex silicon effects and accounting for them in today's design flows.

The Calibre Suite of Tools Offers a Complete Design-to-Silicon Platform

A powerful hierarchical polygon processing engine is at the heart of the Calibre tool suite, which offers a complete design to silicon solution. Each tool is an excellent point tool on its own, but the combination of Calibre DRC, Calibre LVS, Calibre xRC and Calibre RVE (results viewing environment) simplifies and strengthens the design flow. Calibre Interactive provides a seamless, push-button interface, enabling designers to use a single platform for cell/block and

full-chip physical verification. The Calibre manufacturability tool suite for Optical and Process Correction (OPC), Phase Shift Mask (PSM), Scatter Bars (SB) and Off-Axis Illumination (OAI) deliver silicon accuracy, fastest turn-around-time and excellent yield. Calibre MDP allows for seamless continuation of the data manipulations required for mask data format conversion, keeping data hierarchically represented as long as possible.



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