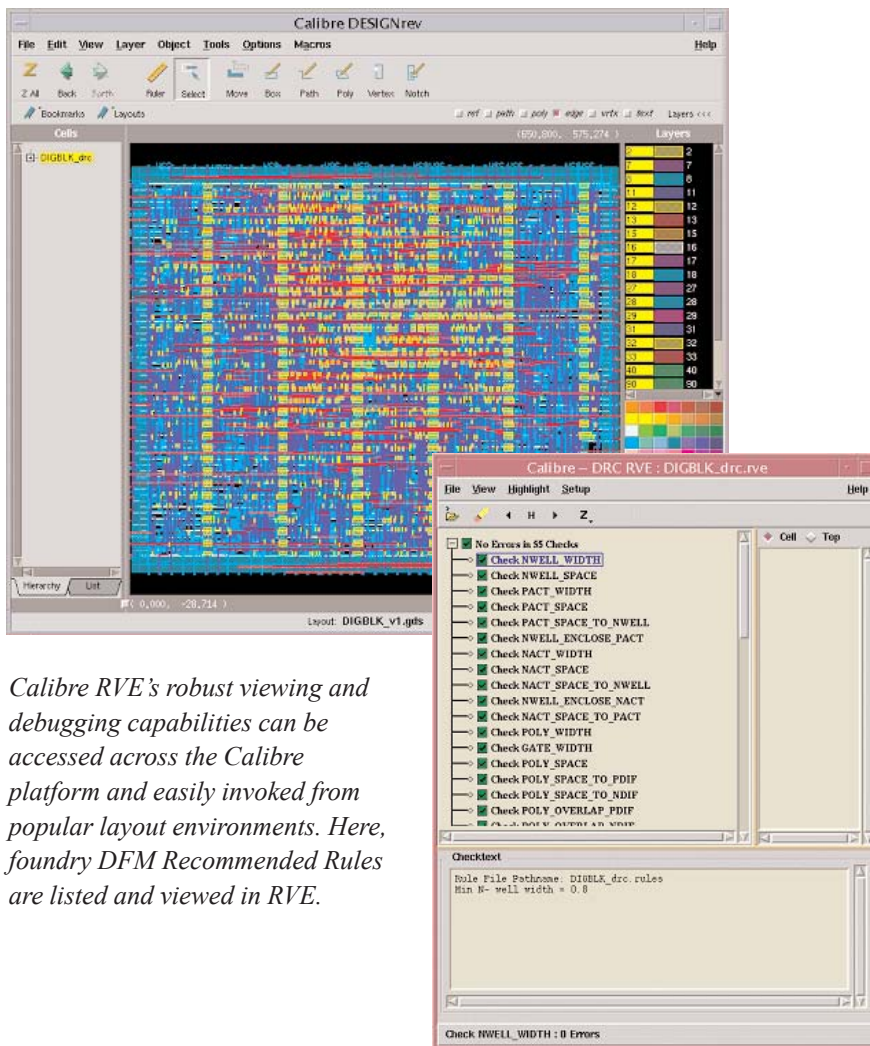


Calibre RVE Results Viewing Environment

Physical Verification

D A T A S H E E T



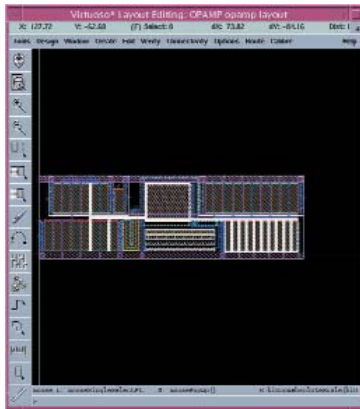
Calibre RVE's robust viewing and debugging capabilities can be accessed across the Calibre platform and easily invoked from popular layout environments. Here, foundry DFM Recommended Rules are listed and viewed in RVE.

Results Viewing Environment: Quick, Intuitive Debugging and Visualization for Design to Silicon Flows

Physical design is a highly iterative process, requiring numerous debug and re-verification cycles. For large deep submicron designs, the total time spent in debug can dramatically impact time to manufacturing. Calibre RVE specifically addresses this problem by identifying design errors instantly in the user's own design environment. It easily integrates into popular layout environments, including Mentor Graphics IC Station and Calibre DESIGNrev, Cadence Virtuoso, Seiko, Synopsys Astro and Enterprise, and more. With Calibre RVE, designers gain a tool that is easy to use and information they need to quickly repair errors.

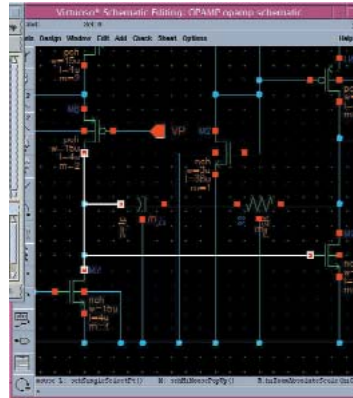
Key product benefits:

- **Save debugging time and iterations for both cell/ block and full-chip designs.** Flexible, customizable interface allows quick, easy selection and sorting of results.
- **Cross probe results** between layout, schematic, source netlist, layout netlist and Calibre LVS result files.
- **View all parasitics generated by Calibre xRC** in the Parasitic Browsing window to see extracted values.
- **Locates and visualizes DFM recommended rules**, working with Calibre DFM tools, DFM Transition, DFM Analyze and DFM Measure.
- **Automated integration into common layout environments** including: Mentor Graphics IC Station and Calibre DESIGNrev, Cadence Virtuoso, Seiko, Synopsys Astro and Enterprise, and more.
- **Highlight to schematic capture products**, including Mentor Graphics Design Architect-IC and Cadence Composer.
- **Automated short isolation debugging** makes even the most complex power ground short simple to fix.
- **Mark Calibre DRC errors** as fixed or waived for subsequent runs.
- **Fast and intuitive hierarchical SPICE browser** for source and layout netlists.

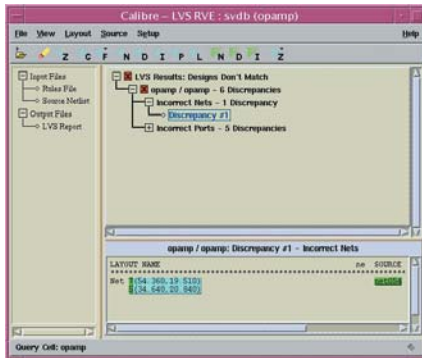


Layout

Schematic



↑ Cross-probe →



Calibre RVE offers dynamic cross-probing capabilities between layout, schematic, source netlist, layout netlist and LVS result files.

Calibre RVE with DRC

- Uses an intuitive graphical user interface to simplify debugging.
- Sorts DRC results by cell or by checks to quickly locate errors in a specific cell, or errors of a specific type.
- Highlights DRC results in context in which they occur, providing flexibility for visualizing the results and determining location of the error and how to fix it.
- Marks results as fixed after correcting the error in the layout. Results marked as fixed are non-persistent.
- Marks results as waived for subsequent DRC runs.

- Exports RVE results to specified layers in the original layout database.
- Designers can generate polygons, such as metal fill, with Calibre DRC and merge it into their original layout database with Calibre RVE

Calibre RVE with LVS

- Highlights LVS results in the layout and schematic windows as well as in the source and extracted netlists, providing designers the ultimate tool for graphical debugging.
- Offers a fast and intuitive hierarchical SPICE browser that highlights nets and devices from the netlist windows. Highlights will appear in layout and schematic windows.
- Uses device highlight filters to control which device types to highlight.

- Uses Include and Exclude window filters to control the area of a highlighted net in the layout window.

- Calibre RVE highlights very large nets in a specified area and uses multiple window filters to further control the highlighted net.

- Uses RVE layer filters to quickly highlight specified layers on any net.
- Offers an Advanced Short Isolation function that can be run hierarchically and by layer. It utilizes a truncation algorithm to minimize the short network, enabling designers to quickly find the result.

Calibre RVE with Parasitic Extraction

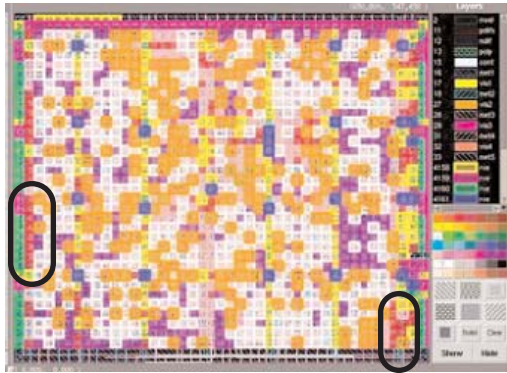
- Uses a Parasitic Browsing window so that designers can easily and quickly see the extracted values of all the parasitics in a simple window.
- Sorts parasitic results by name or by value to quickly find nets of interest or with large parasitic values, or to search for specific nets by name.
- Highlights C, R, and CC results into the layout and schematic windows to help designers identify which polygons in the layout contribute to the parasitic, and where modifications can be made to minimize parasitic effects.

Calibre RVE with RET and MDP

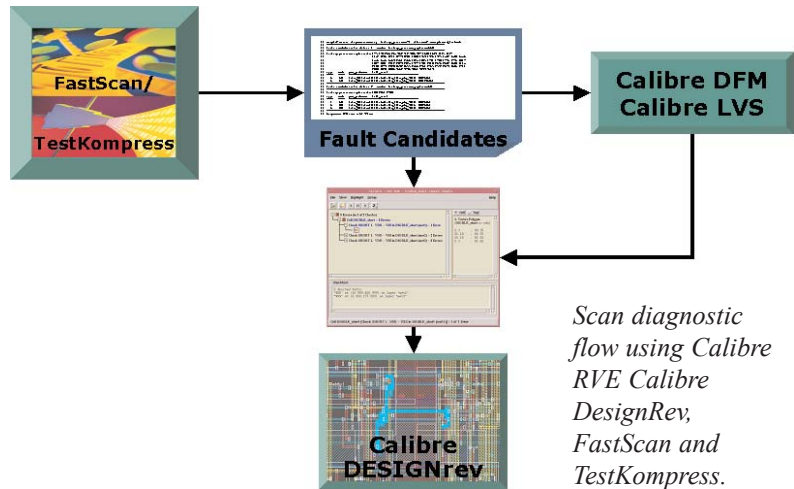
- Allows Calibre ORC (Optical and Process Rule Checking) results to be easily reviewed and fixed. Just click on an error result and see the corresponding layout in a favorite editor tool.
- Allows Calibre MDP (mask data prep) mask rule checking (MRC) problem areas to be highlighted and quickly analyzed or fixed.

Calibre RVE with DFM

Calibre RVE generates histogram plots and colormap overlays based on properties extracted using Calibre DFM (design for manufacturing) tools, including DFM Analyze, DFM Measure and DFM Transition.



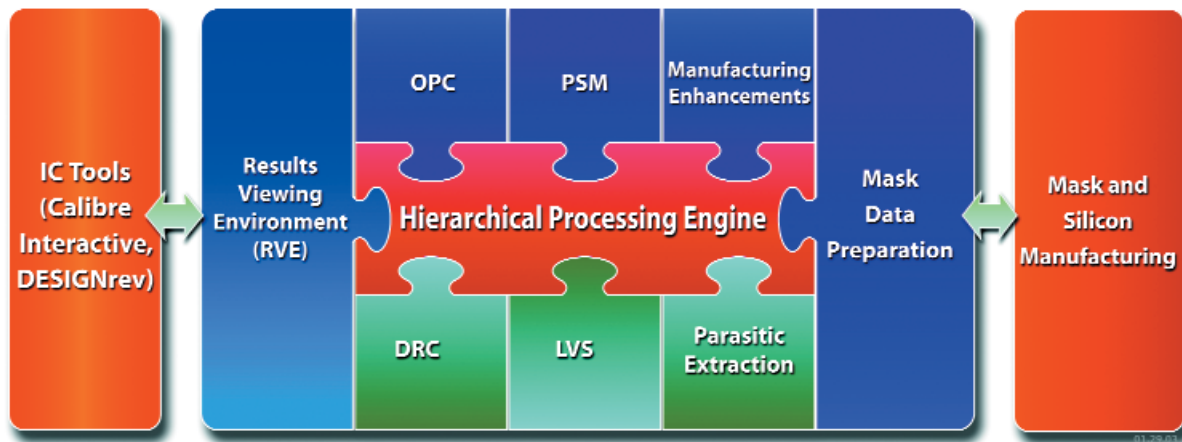
DFM Analyze, visualized through a Calibre RVE feature, identifies the occurrence of yield-limiting layout features.



Calibre RVE with Fast Scan

Calibre RVE works with other Mentor Graphics tools to help locate and visualize issues in designs. Yield management engineers use Calibre RVE and Calibre DESIGNrev to visualize defects located by Fast Scan, the industry leading ATPG tool for at-speed test, diagnostics, and macro testing for small embedded blocks.

The Calibre platform offers a complete design-to-silicon solution to ensure a confident design for manufacturing.



To learn more about Calibre products, visit our website:
http://www.mentor.com/products/ic_nanometer_design/

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