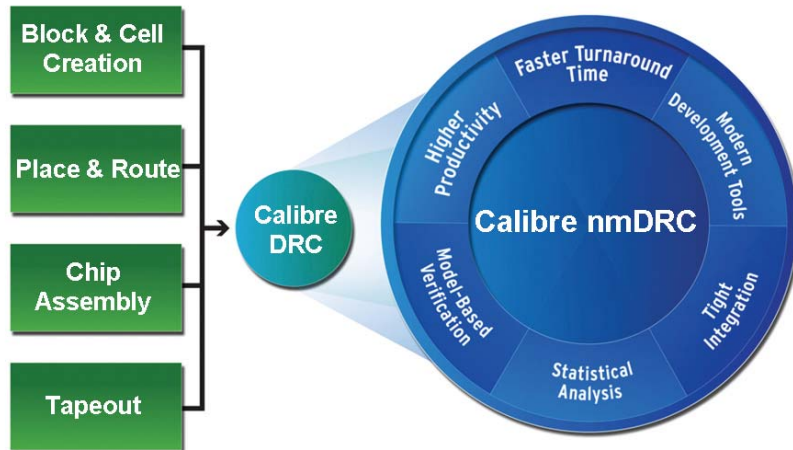


# Calibre nmDRC

D A T A S H E E T



*DRC has changed from the traditional pass/no pass compliance check to a comprehensive methodology that supports multiple analyses, increased performance and scaling, enhanced productivity, and improved cycle times.*

## Evolution of the Calibre Architecture

The Calibre® core processing engine continually evolves to meet the demands of shrinking geometries and complex manufacturing methodologies. While traditional DRC methods of pass/no pass have served well for many years, simple compliance is no longer adequate to account for the variety and complexity of situations that occur in nanometer era processes.

To ensure high yields in nanometer process technologies, designers require new information and new levels of judgment that go beyond design rule checking to include statistical yield analysis. They need new ways to assess the quality of their designs in light of the more complex process constraints and larger process variations they now face.

Mentor Graphics has built upon the industry's production-leading Calibre architecture to create the 5th generation Calibre processing engine. The **Calibre nm Platform** advances the core technology to give designers comprehensive analysis capabilities, and faster run and cycle times. Through **Calibre nmDRC** and improvements in scaling, performance and analysis, designers will be able to manage the hand-off to manufacturing in ways that result in a whole new level of productivity.

## Key Product Benefits

- **Comprehensive sign-off for nanometer designs**, accounting for both compliance and model-based physical verification.
- **Hyperscaling significantly improves runtimes and productivity gains**, and offers advanced data processing options that make efficient use of existing multi-core and distributed processing farms, and extends the useful life of existing capital equipment. Calibre nm is completely compatible with load-balancing software, such as LDF and GRID.
- **Model-based verification enables comprehensive failure analysis in a single robust environment** to determine location of the most significant yield improvement opportunities. Yield metrics are graded by issue, cell and window within the layout tool.
- **Incremental verification** allows designers to begin debugging within seconds rather than hours. Dynamic debugging reduces overall iteration and cycle time, making efficient use of the designer's time.
- **Direct database read/write access** provides back annotation of DFM data into design databases, including GDSII, OASIS, LEF/DEF, MilkyWay and OpenAccess. The OASIS stream file format reduces file size for faster read/write, facilitates file transfer and data storage.
- **Tel Verification Format (TVF) rule file support** significantly reduces code input, simplifying the development and maintenance of advanced rule files.

## Calibre nmDRC Hyperscaling for Dramatic Runtime Improvement

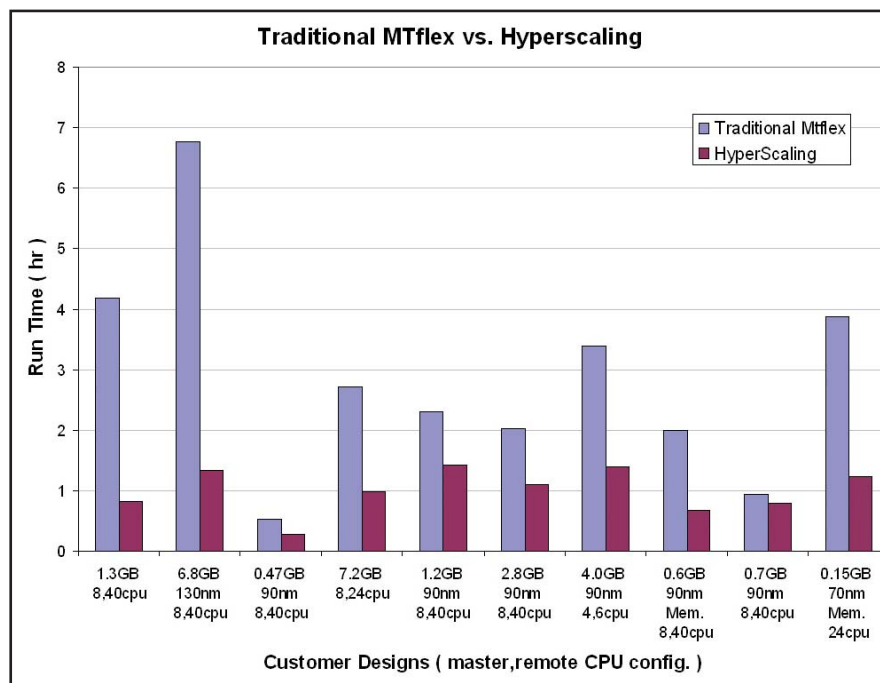
With increasing size and complexity of designs, and the explosion of new rule checks required for the next technology node, the need for faster turn-around-time (TAT) is critical.

**Calibre nmDRC Hyperscaling** extends Calibre's production-proven performance architecture to significantly increase scaling and reduce TAT. Hyperscaling runs in either central or distributed shared memory processor environments, such as 8-way Opteron or EM64T Linux boxes. Allowing continued use of existing equipment saves design teams additional capital expenditures.

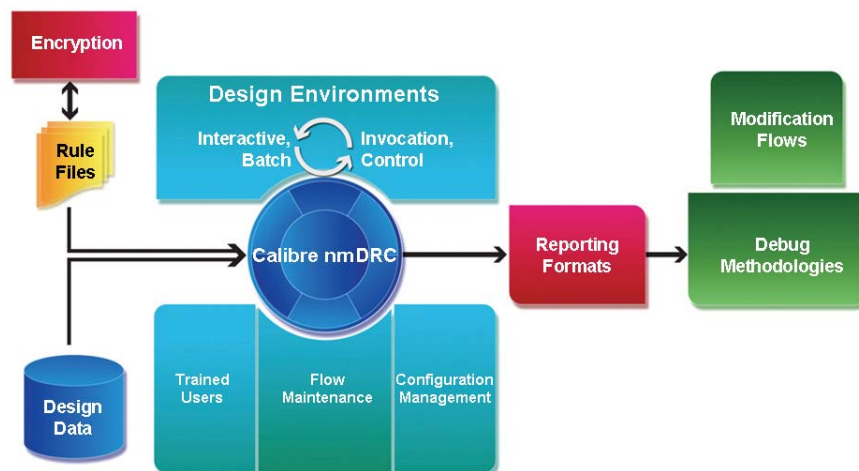
Design verification is much faster using existing hardware. Users can gain even greater improvement on new or additional hardware. Cell block verification jobs can be run in parallel as multiple designers work to complete subsections of a design on the same hardware, which is tied together for full chip verification. Performance and TAT goals can be achieved or exceeded at a fraction of normal cost.

Hyperscaling also provides productivity improvements with no changes to current SVRF decks, protecting investments in deck development and staff expertise. SVRF decks created years ago, as well as the most advanced 45nm decks, run faster. Calibre nmDRC is completely compatible with load-balancing software, such as LSF and GRID.

Hyperscaling improves performance whether designers are working in 180nm designs or 45nm designs.



Calibre's new architecture enables a Hyperscaling mode that provides fast turn-around-time on distributed hardware. Hyperscaling improves scaling to as much as 40X on existing equipment and continues scaling out to 100 CPUs. Even on 8 CPUs, DRC runs have improved from 5x scalability to 8x. On 24-CPU machines, the scalability is still nearly linear, up to 23x. In the graphic above based on customer benchmarks of Calibre MTflex vs Calibre nmDRC with Hyperscaling, Hyperscaling has dramatic productivity gains, with an average of 2.9X improvement. The four largest designs gained a 3.8X runtime improvement.



Calibre nmDRC drops into the designer's current CAD environment without disruption or risk. Users can immediately realize new functionality and dramatic total cycle time improvement within existing infrastructure.



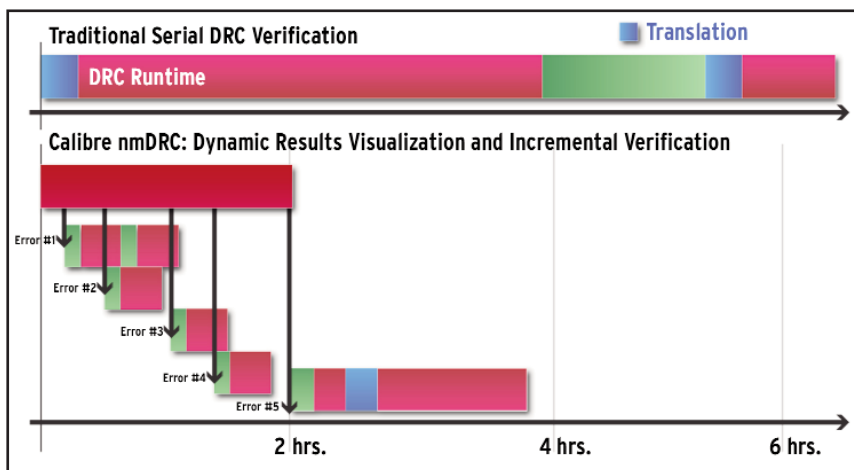
## Incremental Verification

Incremental verification fundamentally changes the iteration process. In traditional methods, a designer must wait until the DRC run is completed before beginning the debug process. Incremental verification allows designers to begin debugging immediately during the run time, as soon as the first error is identified.

Calibre nmDRC automatically identifies changed regions (shown in the graphic at right), reads only the changed areas and runs only the effected checks. Calibre nmDRC also eliminates translation time, allowing further reduction of overall cycle time and giving designers the option of performing several run/debug cycles in a single day.



*Calibre nmDRC identifies error regions, then reads only the changed areas, dramatically reducing cycle time.*



**Incremental DRC**, representative of all Calibre nmDRC improvements (Hyperscaling, Incremental Verification and Direct Database Read), does not require translation, shortens iteration time through concurrent debugging and DRC runs, and improves productivity. The entire physical verification cycle can be completed in less than a day. The traditional six-hour DRC cycle time permits only one complete cycle in a day. It may afford enough time to get a second debug cycle started, but no more.

## The Calibre nm Platform

The industry standard Calibre platform from Mentor Graphics offers a complete solution that bridges design-to-manufacturing. It provides a data communication link crucial to improved yield and reliability in nanometer IC designs. Fueled by a single, powerful polygon processing engine, the Calibre nm Platform includes solutions for physical verification, parasitic

extraction, resolution enhancement, mask data prep, litho-friendly design, and design for manufacturing.

Complete Calibre rule files and extensive coverage of the nanometer processes for DRC and DFM are available at a majority of the world's semiconductor foundries, including Chartered, IBM, Jazz Semiconductor, TSMC, and UMC. Calibre is the physical verification standard used internally by Chartered, TSMC and UMC.

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