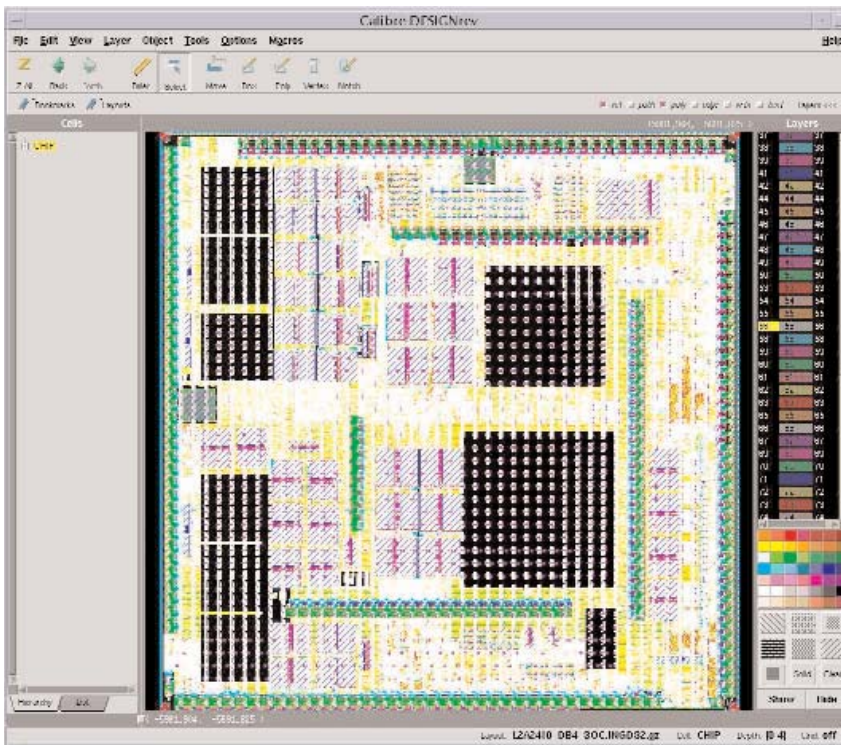


Calibre DESIGNrev

Physical Verification

D A T A S H E E T



Calibre DESIGNrev loads and displays multiple gigabyte GDSII and OASIS stream files in just minutes. Robust chip finishing capabilities allow full chip designers a method for merging, creating, verifying and comparing full chip data.

Robust Chip Finishing and Rapid Full-Chip Viewing

For engineers integrating and assembling complete chips, the process of going from first pass integration to successful tape-out can be lengthy and difficult. With design size and complexity increasing, traditional layout editors lack the capability to quickly and efficiently visualize, revise and stream-out layout data. Performing simple tasks on large full-chip GDSII and OASIS files, and preparing the design for the mask manufacturing process (chip finishing), often can take hours, delaying tape-out. Calibre DESIGNrev speeds full-chip design completions and tape-outs by rapidly loading, displaying and saving large GDSII and OASIS files. Chip finishing can also be quickly performed in DESIGNrev, giving designers the capability to merge actual cell representations of abstracts, place logo cells, replace vision cells, create seal rings, perform metal fill and via insertion, add critical dimension (CD) patterns, add corner stress relief patterns, modify polygon, cells and more in post verification, compare original data to modified version, and verify trace net connections. In addition, Calibre DESIGNrev allows engineers to quickly zoom to regions of interest, identify and fix physical verification errors, and conveniently re-invoke Calibre DRC and Calibre LVS.

Key Product Benefits

- **Opens Multi-Gigabyte GDSII Files in Minutes:** Current benchmark tests prove DESIGNrev opens and loads files at *1Gb per minute*, dramatically reducing time to tape-out.
- **Chip Finishing Solution:** DESIGNrev provides a robust method for chip finishing, with the capability to merge actual cell representations of abstracts, place logo cells, replace vision cells, create seal rings, perform metal fill and via insertion, modify polygon, cells and more in post verification, compare original data to modified version, and verify trace net connections.
- **Robust Revision and Iteration Loop Capabilities:** Calibre DESIGNrev offers quick viewing, error identification, modification and re-invocation. Includes cut, copy, paste, delete, move and more with unlimited undo/redo function.
- **Customizable Macros:** Calibre DESIGNrev supports the open standard tcl/tk macro language for extensive tool customization.
- **Accesses Native Data:** Calibre accesses data within the GDSII or OASIS database, including polygons, edges, text, cells, instances, arrays and more.
- **32- and 64-bit Support:** Support for Hewlett-Packard, Sun Solaris and Linux operating systems.

Chip finishing capabilities

Chip finishing prepares a design for the manufacturing process. Finishing is performed within the original design data and GDSII before being handed over for mask making. Within Calibre DESIGNrev, designers can merge data (actual cell representations of abstracts, placement of logo cells and revision cell replacement), create data (seal rings, metal fill, via insertion, post verification modifications), and verify and compare data (post layout verification, XORs, trace net connections) at the full chip level. Because of design sizes, older tools took as long as 2 days to complete the chip finishing process. With Calibre DESIGNrev, the process can take as little as 2 hours.

Fast Tape-Out

The full chip debugging process can be lengthy and hard to manage. Chip size has outgrown the ability to do revisions in layout editors. With older tools it can take as long as 8 hours to open a

2 gigabyte GDSII or OASIS file.

Standard visualization steps (pan, zoom) are slowed by large databases and stream-out can add hours of waiting time.

Alternative methods have not solved the problem. Place-and-route tools lack robust revision capabilities. Database management is also difficult; edits made in proprietary databases are not always captured in the final GDSII. GDSII viewers speed visualization, but do not allow revision or correction.

Unlike other viewing tools, Calibre DESIGNrev lets users manipulate native GDSII and OASIS database objects, such as cells, instances, polygons, edges and text, with standard revision capabilities: cut/copy/paste, add, delete, move and break.

Calibre DESIGNrev offers the best and fastest solution for debugging large files and keeping tape-out on schedule.

Integration with Calibre tools

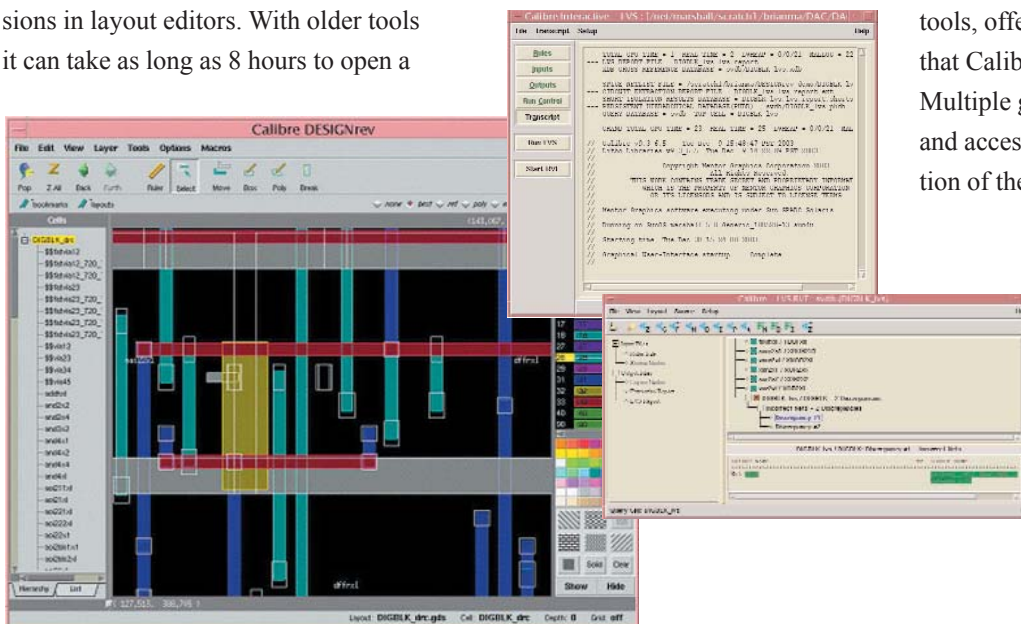
Through tight integration with Calibre RVE, Calibre DESIGNrev offers quick error identification and cross-probing capabilities. When coupled with Calibre Interactive, Calibre DRC and Calibre LVS are easily invoked. Users can verify and reverify the entire design or only the portion of the design just modified.

Customizable tcl/tk macro support

Calibre DESIGNrev supports the open standard tcl/tk macro language, giving users the ability to customize the tool to their requirements. Leveraging upon this capability is a library of previously defined macros that call up commonly used Calibre DRC functions.

Fueled by the high-performance Calibre polygon engine

Calibre DESIGNrev is part of the Calibre family of design-to-silicon tools, offering the speed and capacity that Calibre users are accustomed to. Multiple gigabyte files can be opened and accessed in minutes using a fraction of the same dataspace in RAM.



Through tight integration with Calibre RVE, Calibre DESIGNrev offers quick visual error identification and cross-probing capabilities.

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