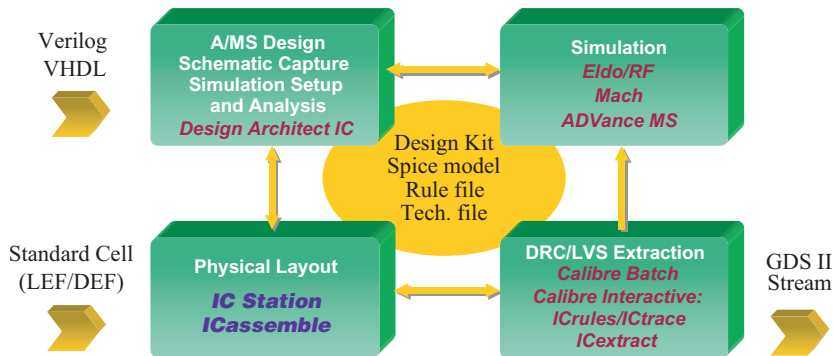


IC Station Tool Suite

Mentor Graphics Analog/Mixed-Signal Design Flow



The IC Station® Tool Suite provides the physical layout component of the Mentor Graphics full custom IC design flow. This suite includes application bundles for editing, schematic-driven layout, and top-level floor planning/routing.

A Total Design Solution

Integrated circuit design is becoming more complex every day. This is especially true in analog and mixed-signal design. To address critical time-to-market issues as designs become increasingly complex, Mentor Graphics has developed a complete analog/mixed-signal IC design flow, from schematic capture to physical layout and verification. With the help of foundry partners, we deliver complete design kit support for your target process technology, ensuring immediate access to essential data. And all of the tools in the Mentor A/MS flow are Linux compatible, so you can make computing environment choices based on your unique cost/performance needs. That's why analog/mixed-signal IC designers who need a total design solution choose the Mentor Graphics IC Station Tool Suite.

Major product benefits:

- Improves layout design throughput up to 50X compared to manual layout methods
- Reduces design rule checking (DRC) debugging cycles, leading to shortened time-to-market
- Verifies DRC and layout vs. schematic (LVS) correctness throughout the layout process, without adding complicated steps
- Creates DRC-correct complex layout with a simple command to improve reliability of final product
- Lowers capital equipment costs by utilizing cost-effective Linux workstations
- Enables changes to layout based on updates to the schematic at any point in the design cycle
- Enables layout designers to manage very large databases without resorting to special design methodologies

Key product features:

- Schematic and/or SPICE netlist-driven layout and flow
- On-the-fly DRC while performing standard editing commands
- Integrated Calibre® DRC and LVS checking within the layout editor
- Ready-to-use parameterized device generators for digital and analog layout design
- Operates on Linux OS with full UNIX data compatibility
- Integrated Engineering Change Order (ECO) component
- High-capacity database editing
- LEF/DEF interface

Analog/Mixed-Signal IC Design

The IC Station Tool Suite offers an easily configured, affordable option for physical design engineers who need increased productivity and an immediate, automated way of handling the physical layout of their A/MS designs. Design engineers can be fully functional with the IC Station tools in as little as one day, without incurring additional consulting charges.

The IC Station Tool Suite consists of three application bundles:

- **ICgraph Basic**
- **IC Station SDL**
- **ICassemble**

These bundles are offered in a standard configuration, with optional applications available based on the design engineer's unique requirements. And with Mentor Graphics, users can be assured they will receive the highest level of support in both training and technical assistance.

ICgraph Basic

ICgraph Basic supports an extensive set of editing functions for efficient, accurate polygon editing. This gives the design engineer full control of circuit density and performance, while improving productivity by as much as 5X to help meet time-to-market objectives.

Hierarchy and advanced window management allows multiple views of the same cell, providing the capability to edit both views. And with ICgraph Basic, design engineers can create matched analog layouts quickly by editing using a half-cell methodology.

- ICgraph Basic features a flexible license manager, which gives users

the ability to efficiently manage their license pools, resulting in greatly reduced license costs.

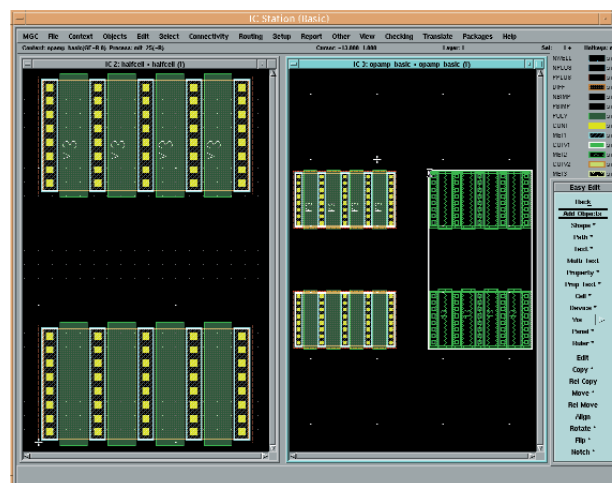
- The high capacity database enables design engineers to manage very large databases without having to resort to special design methodologies. ICgraph Basic enables users to manage databases up to and over 2Gb.
- The Linux version of ICgraph Basic gives users the ability to edit on cost-effective Linux workstations.
- GDSII read/write performance offers the fastest available file access.
- Move as close as possible (Move ACAP) feature enables design engineers to manipulate layouts from coarse grid resolutions or large layout views, reducing the number of steps in the layout process and increasing productivity.
- The ASCII layout database translator enables complex customization for executing batch commands from within a UNIX/Linux environment, allowing users to meet all their design needs with one tool.

IC Station SDL

Schematic-driven layout (SDL) is a design methodology that enables physical design engineers to create IC layouts based on information from a logic source. IC Station SDL enables automated creation of layout data, while maintaining the relationship between layout and schematic, reducing design cycle time and assuring correct-by-construction layout. Any mix of polygons, device generators (either custom or built-in), and cell data are supported in the layout environment.

IC Station SDL helps bridge the gap between schedule and performance goals, offering productivity increases of up to 50X over traditional manual layout methods. This powerful set of tools includes all of the functionality of ICgraph Basic, along with a hierarchical, schematic-driven layout environment, enabling design engineers to quickly create complex designs without sacrificing layout quality.

- Using schematic-driven layout, design engineers can 'pick and place' devices either automatically or graphically. The dynamic connectivity display with cross probing



Editing using a half-cell methodology, design engineers can create matched analog layouts quickly and easily.

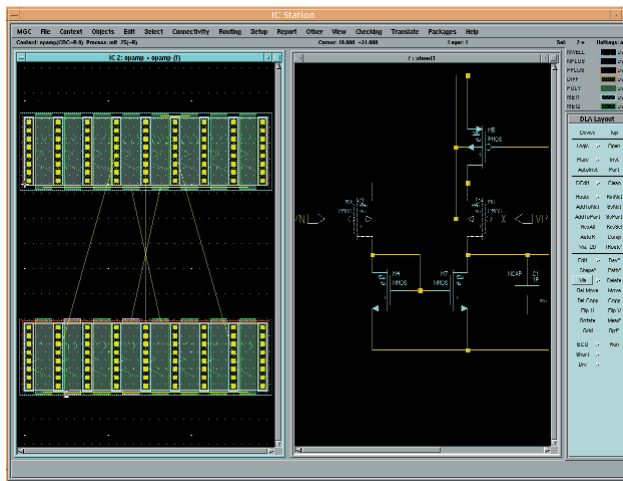
makes navigation between the layout and schematic fast and easy.

- The Engineering Change Order (ECO) component quickly modifies the layout to reflect schematic-driven engineering changes throughout the design cycle. After comparing the layout with the logic source, ECO automatically implements design

automated area reduction using Calibre DRC rules. Semi- or fully automatic compaction allows layout designers to increase productivity without sacrificing layout area. During the design cycle, connections and placements can be created faster at loose constraints; then the layout can be post-processed to achieve tight area constraints.

that are logically correct and design rule-compliant, resulting in dramatic increases in productivity over traditional manual layout methods.

Devices can also be added and modified manually through the use of forms and interactive editing commands. IC Station SDL speeds the creation of design rule-correct parameterized devices, resulting in design rule-correct layouts.



Schematic-driven layout enables designers to 'pick and place' devices either automatically or graphically.

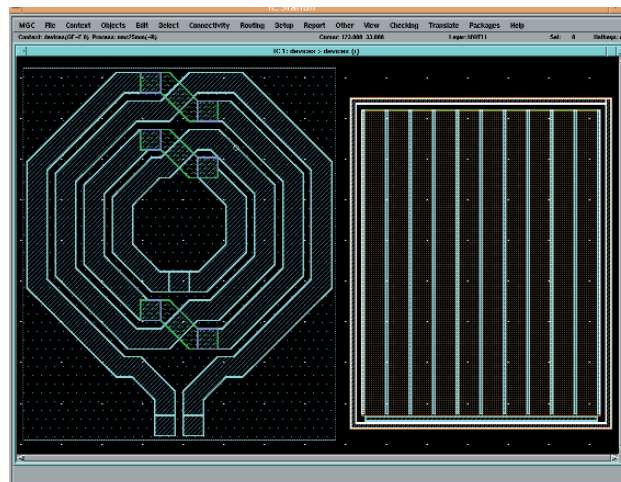
changes in the layout and optionally corrects additions, deletions and property changes, reducing the time required for layout revisions.

- Short checking functionality enables design engineers to find potential shorts caused by overlapping nets before running LVS.
- Design engineers can view the shorts in a browsing menu and make necessary changes.
- Connectivity enables the representation of accurate layout connections at all times in the design cycle. Using connectivity throughout the design process guides designers in creating LVS-correct layout, shortening LVS debug cycles.
- The compaction feature supports

Automated Device Generation

IC Station SDL includes ready-to-use parameterized device generators for digital and analog layout design. With IC Station SDL, design engineers can utilize information stored in the logic source to automatically create devices

- Parameterized layout allows standardization across multiple users and sites for design, creating DRC-correct complex layouts with a simple command, leading to improved reliability of the final product.
- The transistor device enhances productivity for all designs, including complex memory designs using bent gates. Transistor editing commands offer enhanced flexibility for intricate designs without destroying the device, improving productivity and reliability.
- The capacitor device creates standard capacitors as well as complex switch capacitors, with a single command, for increased productivity.



Automatic device generation speeds the creation of parameterized devices that are design rule-correct.

- The shape-based capacitor device allows layout designers to 'fill' areas with capacitors for area savings, and increase flexibility for future design changes.
- The via device allows design engineers to quickly create power rail connections with one simple command.
- The resistor device supports multiple processes, as well as series and parallel structures. Creation of matched resistors is accomplished with a single command.
- The guard band device enables design engineers to quickly shield sensitive analog layouts. Guard band editing commands include the ability to cut, in order to complete routing to sensitive analog layouts, increasing productivity.

Advanced floor planning features:

- Multiple area estimation modes
- Layout wire propagation (push/pull through hierarchy with connectivity)
- Simple hierarchy management
- ECO flow integration
- Top-down block boundary editing ability
- Input from Design Architect-IC schematic, SPICE netlist, Verilog netlist
- Read/write LEF/DEF blocks

Interactive routing capabilities:

- Truly integrated routing technology with pushing for "routing in place"

- Flexible blockage control
- On-the-fly visual feedback of length, resistance, capacitance, or costing
- Intelligent minimization of nets being pushed
- Multiple bus routing modes
- Shielded wires
- Mirrored and differential pair routing
- Controlled wire handling for timing closure
- Supported post-routing functions:
 - Via minimization
 - Layer swapping
 - Wire bend reduction

ICassemble

As the digital content in today's mixed-signal SoC designs continues to grow, top-level floor planning and routing is becoming an increasingly important component of the design flow. To address the complexities of analog/mixed-signal chip assembly, Mentor Graphics developed ICassemble, which provides a robust set of features for floor planning, top-level assembly and interactive routing.

Use common centroid analog layout methodology for speed, ease and higher yields.

Visit our website at www.mentor.com/cicd for the latest product news.

Copyright © 2001 Mentor Graphics Corporation. Eldo, ADVance, ICview, ICgraph, ICdevice, ICplan, ICblocks, ICcompact, and Mach TA are trademarks and IC Station, Falcon, Design Architect, HotPlot and Calibre are registered trademarks of Mentor Graphics Corporation. All other trademarks mentioned in this document are trademarks of their respective owners.

Corporate Headquarters
Mentor Graphics Corporation
8005 SW Boeckman Road
Wilsonville, OR 97070-7777
Phone: 503-685-7000

Sales and Product Information
Phone: 800-547-3000
503-685-8000

Silicon Valley Headquarters
Mentor Graphics Corporation
1001 Ridder Park Drive
San Jose, California 95131 USA
Phone: 408-436-1500
Fax: 408-436-1501

North American Support Center
Phone: 800-547-4303
Fax: 800-684-1795

Europe Headquarters
Mentor Graphics Corporation
Immeuble le Pasteur
13/15, rue Jeanne Braconnier
92360 Meudon La Forêt
France
Phone: 33 (0) 1-40-94-74-74
Fax: 33 (0) 1-46-01-91-73

Pacific Rim Headquarters
Mentor Graphics (Taiwan)
Room 1603, 16F
International Trade Building
No. 333, Section 1, Keelung Road
Taipei, Taiwan, ROC
Phone: 886-2-87252000
Fax: 886-2-27576027

Japan Headquarters
Mentor Graphics Japan Co., Ltd.
Gotenyama Hills
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140
Japan
Phone: 81-3-5488-3030
Fax: 81-3-5488-3021

Mentor Graphics®



Printed on Recycled Paper

6-01 HDG

1017090