

# VStationPRO

## High-Performance System Verification

## System-Level Verification

## D A T A S H E E T



*High-capacity, high-performance functional verification solution for complete System-on-Chip validation.*

### VStationPRO Empowers Functional Verification

VStation™PRO from Mentor Graphics is the sixth generation VStation product. It offers a complete environment that provides all the power required to verify complex designs from 1.6 to 120 million gates. VStationPRO is founded on the successful VirtualWires technology, ideally suited to demanding applications such as 3G wireless, multimedia graphics, and hardware/software verification of embedded processors. VStationPRO supports RTL and gate-level verification up to 1 MHz performance in a simulation-like debug environment that allows 100 percent signal visibility into the design. Mentor has a host of real-time verification solutions that including leading edge interfaces like PCI Express, ARM 946 cores, and 3GPP interfaces. VStationPRO links with the Seamless® co-verification environment for concurrent hardware and software verification. VStationPRO handles true asynchronous clock behaviors to ensure model fidelity and verification accuracy. VStationPRO delivers high-capacity, real-system verification and the confidence that designs are correct prior to committing to fabrication.

### Major product features:

- Scalable capacity from 1.6 to 120 million gates
- Up to 1 MHz verification performance
- Memory capacity of 16 to 576 Mbytes
- Compile rate of 5M gates/hour
- Supports flexible use modes
- Mixed-language, VHDL, and Verilog compatibility
- RTL and gate-level verification
- RTL source-level debug and view
- 100 percent visibility into design
- HW/SW co-verification with ARM7, ARM926, TI DSP, IBM PowerPC
- Multimedia graphics for MPEG, RGB, PCI Express, AGP, and PCI64
- Wired and wireless networking interfaces including ethernet and 3GPP
- Based on VirtualWires™ proven technology
- Highly reliable, stable platform

## Fully Automatic Partitioning and Compilation

The VStationPRO VirtuaLogic™ compiler is entirely automatic, requiring significantly less user intervention during the compile and design bringup phase as compared to competitive solutions. Based on the patented VirtualWires technology, VirtuaLogic provides highly reliable compiles by isolating any timing and modeling issues of the underlying hardware. VirtualWires is a production-proven technology that scales well beyond the capacity of the present VStationPRO. The VirtuaLogic compiler guarantees that a design will behave in the intended manner regardless of the VStationPRO instance used.

## Powerful Debug and Analysis

The VStationPRO 100 percent visibility feature and simulator-like debug environment maximizes verification productivity, allowing designers to quickly isolate problems hidden in complex designs. Using a patented software technique, the 100 percent visibility feature allows users to view every signal in the design without recompiling. A new probing and data sampling architecture integrates the logic analyzer functionality within the array boards, making it scalable with the system.

VStationPRO allows the designer to stay in the RTL domain while debugging the design. Multiple, dynamically-linked windows provide a comprehensive test environment and visibility into every detail of the design. In addition to the waveform window, the source window provides a textual display of the design, while the hierarchy window displays the design structure and data flows between design blocks. The actual signals can be viewed in various formats separately or simultaneously.

## High Speed RTL Compiler

The RTL compiler accelerates verification turnaround time with extremely fast compile times. The RTL compiler enables a direct mapping of the design written in RTL onto the FPGAs in the VStationPRO without a separate, time-consuming synthesis step. Bypassing synthesis also allows the RTL compiler to maintain signal name integrity and design hierarchies. This capability allows the user to debug the design at the RTL using the VStationPRO familiar and easy-to-navigate, simulator-like user interface. VStationPRO's advanced RTL debugging capabilities include source code debugging with active line and break pointing, a graphical path browser, and a waveform viewer, all dynamically linked to maximize debug productivity.

Array Board	
Modularity	1.67M, 3.33M, 6.67M gates/board
ASIC Gate Capacity	1.67M–120M gates
Memory Capacity	16–576 Mbytes
Emulation Speed	500 kHz to 2 MHz
I/O Connections	512–4608
Probing	13,000–120,000
Dimensions	21.5 in. wide x 36 in. long x 27.5 in. high (54.61 cm x 91.44 cm x 69.85 cm)
Weight	Chassis weight with 1 system board 320 lbs. (145.45 kg) Array board weight (each) 30 lbs.(13.64 kg)
Power	186–264 VAC, 47–63 Hz, 280 VA
TIP Interface	32-bit PCI interface for SUN Blade 1000
Recommended Host Workstation	SUN Blade 1000 with 16 bit wide fast SCSI, Solaris 8

## Visit our website at [www.mentor.com/emulation](http://www.mentor.com/emulation)

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