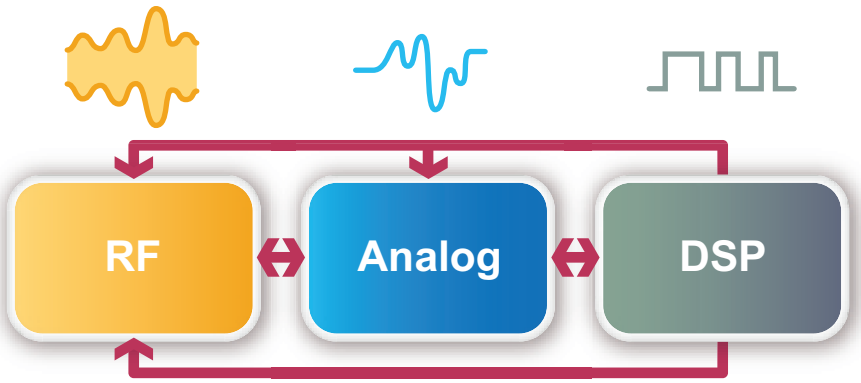
ADVance MS RF



The interaction between RF blocks, analog baseband and digital baseband subsets of modern RF systems is becoming tighter. In many cases, the verification of these interactions is just impossible, putting first silicon at risk of failure. ADMS RF is a unique simulation solution for efficient verification of such circuits. ADMS RF provides 100x or 1000x speedup ratios over regular time-domain simulation.

Major Product Benefits:

- **More complete verification of complex RF SoCs for wireless communication applications minimizes risk of faulty RF/ baseband connections.**
- **ADMS RF simulates complete systems orders of magnitude faster than previous tool generation. More operating conditions can be verified.**
- **ADMS RF preserves transistor-level accuracy wherever it is necessary. Simplifications, such as behavioral modeling, are left entirely to the user's initiative.**
- **ADMS RF uses industry-standard languages only, and no proprietary languages. Reuse of unmodified legacy code is facilitated.**
- **RF and baseband IC designers can start working together, with the same tools, much earlier in the design process. Productivity is enhanced.**

Complete Verification of RF-DSP Systems

Integrated RF and Mixed-Signal Simulation

Complete simulation of RF Systems-on-Chip (SoC) becomes a reality with the inclusion of Eldo™ RF capabilities into ADVance MS™ (ADMS). The ADVance MS RF (ADMS RF) solution can simulate communication systems containing tightly-linked RF and baseband functions—analog and digital—in the most effective way.

ADMS RF

ADMS RF allows the simulation of systems integrating an RF front-end and baseband functions with complex digital signal processing (DSP) in VHDL or Verilog. Direct conversion receivers or amplifiers with high-speed digital automatic gain control (AGC) are simple examples. Verifying such systems requires simultaneous, transistor-level simulation of the RF part with the baseband part in acceptable CPU times.

Building upon Solid Foundations

About ADVance MS

ADVance MS is an industry-leading tool for mixed-signal simulation. Complex mixed-signal chips can be verified with all their analog-digital connections. It is a language-neutral environment including SPICE, VHDL, Verilog and standard analog behavioral languages such as VHDL-AMS and Verilog-AMS.

About Eldo RF

Eldo RF efficiently simulates the RF blocks in typical RF transceivers, such as low noise amplifiers, mixers or voltage controlled oscillators. It features high-performance RF-specific algorithms such as the steady-state analysis and the modulated steady-state analysis (MODSST). This provides the necessary simulation speedup for these critical blocks operating at the highest frequencies, typically several GigaHertz.

ADMS RF— How does it work?

ADMS RF runs in a mode where the MODSST algorithm of Eldo RF is used in place of the regular transient algorithm of ADMS. The circuit can be described with any mix of SPICE, Verilog-AMS, Verilog and VHDL.

The MODSST algorithm is a mixed time-frequency algorithm which computes a time-varying spectrum. At discrete time points, the spectrum of the signals is computed using the steady-state analysis of Eldo RF. The spacing of time points is chosen to follow the slow-varying baseband information, rather than the fast-varying RF carriers.

This results in speedup ratios over regular transient simulation. Two or three orders of magnitude are usual figures with the typical baseband-to-carrier frequency ratios in wireless networks (WLAN) applications for example.

Single Kernel Architecture for RF-DSP simulation

ADMS RF is an extension to the single-kernel architecture of ADMS, and thus greatly simplifies the use of its complex underlying algorithms.

This architecture departs from 'co-simulation' approaches where simulators are glued together using limited and cumbersome interfaces.

Users can concentrate on design issues rather than simulator issues. The usual ADMS user interface is left unchanged. Simply, the Eldo RF MODSST analysis is used in place of the usual transient analysis.

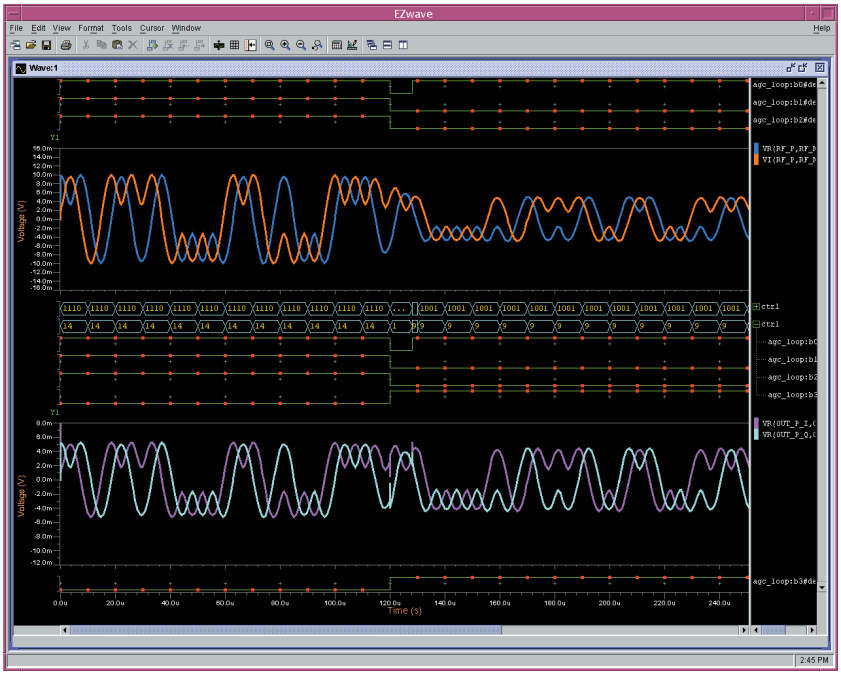
Transistor-level Accuracy

ADMS RF differs from so-called system-level approaches, which rely on crude behavioral modeling based on proprietary languages, or even simple linearization of the fast-varying RF signals. ADMS RF retains the full accuracy of circuit-level simulation, where and when desired by the user.

The critical RF blocks can be described at the transistor-level (SPICE), so that all high-order effects are still captured (foundries deliver device model parameters for Eldo, based on the Bsim3, Bsim4, VBIC or HICUM standards). For increased performance, less critical RF or analog blocks can be described in Verilog-AMS, and the DSP content in Verilog and/or VHDL.

Digital Modulation for all Wireless Standards

To simplify simulations in the context of wireless standards, ADMS RF supports all common digital modulation formats, such as GMSK, QPSK, QAM, GFSK, EDGE, HPSK, OFDM



etc. Built-in sources deliver signals modulated according to these schemes, including the standard baseband filters such as Root Cosine or Gaussian filters. The input signal can be either explicit binary sequences, or CCITT-compliant PRBS sequences.

Measurement functions allow the estimation of critical figures of merit such as ACPR, EVM or BER.

Maximize Re-Use for More Productivity

ADMS RF uses industry-standard languages only: SPICE, VHDL, Verilog and Verilog-AMS. Reuse of legacy code is thus greatly simplified. An existing ModelSim® design can be imported in a matter of seconds, without any modifications, and simulated along the transistor-level mixers and VCOs of the RF front-end, whatever the feedback and control loops.

ADMS RF is integrated in the Mentor Graphics IC Flow and in the Cadence ADE framework.

Summary of Key Features

- Uses SPICE, VHDL, Verilog, Verilog-AMS.
- Integrated RF and mixed-signal baseband simulation.
- Reuse of HDL legacy code.
- Critical RF blocks can be described with BSIM3, BSIM4, HICUM and other standard device models.
- Behavioral RF modeling in Verilog-AMS.
- Efficient time-frequency domain simulation with multi-gigahertz carrier frequencies.
- Integrated in the Mentor Graphics IC Flow and the Cadence ADE environments.
- Familiar ADMS interface for a shorter learning curve.

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