

Tau presents timing violations in an easy to interpret spreadsheet that is integrated with waveform views of the data.

Major product benefits:

- Comprehensive worst-case timing analysis and verification
- Generate routing constraints to drive physical design
- Eliminate false timing violations with symbolic timing analysis
- Easy to use spreadsheet-based user interface and model development tools
- Timing models are easily created for general use in multiple designs
- Interfaces with most popular CAD systems

Symbolic Timing Analysis

The Tau[®] board-level symbolic timing analysis tool performs comprehensive worst-case timing analysis and verification on designs using an advanced symbolic timing methodology, eliminating false paths that are typically reported in standard static timing tools.

Tau employs models that contain both timing and functional information. By exploiting this combination, Tau restricts analysis to timing paths that are truly relevant, thus facilitating analysis and verification without the need for test vectors.

Skew and phase shift between clocks is automatically computed within Tau by traversing the clock tree. Delay correlation within a single component eliminates overly conservative, worst-case (min./max.) timing analysis.

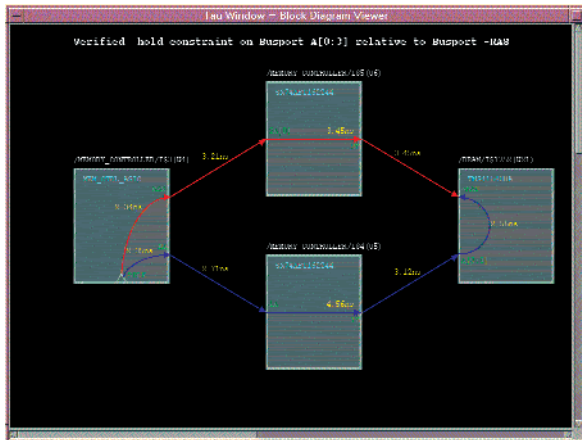
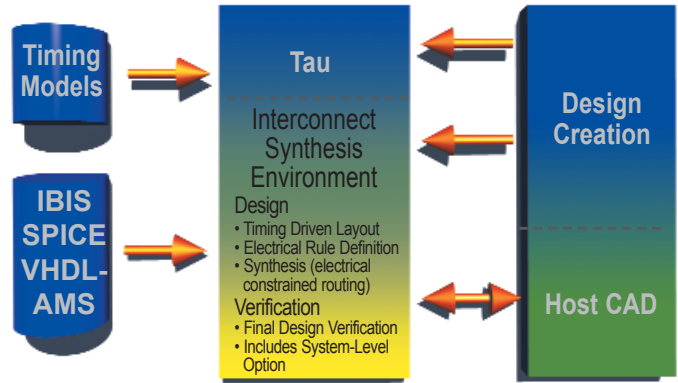
Models

An easy to use, fully integrated model development tool is provided, allowing manual creation and modification of Tau models. In addition, interfaces are provided to allow automatic import and creation of timing information for custom components such as FPGAs, ASICs and EPLDs. Support for multiple industry standard modeling formats, such as STAMP, Timing Diagram Markup Language (TDML) and Timing Designer Files allow the direct import of timing and functional information to further simplify the model creation process.

Integration with Physical Design

Routing Constrains are exported from Tau for use within the Interconnect Synthesis (ICX) family of products. This enables the timing driven floor-planning and timing driven routing capabilities of the IS tools to use constraints created from the actual design.

The IS_Analyzer™ and the IS_Floorplanner™ tools generate accurate interconnect delay results, based on transmission line simulations across multiple corners. Tau is able to import simulated interconnect delays for analysis of the complete timing path with interconnect considerations. Interconnect delays from the ICX tools can be imported at any stage of the design process: during placement, initial routing or final routing. The combination of ICX and Tau provide a complete timing and Signal Integrity verification solution.



Tau's block diagram view shows critical timing paths, including the actual delay values and any timing constraint violations.

Minimum Requirements

Mentor Graphics recommends the following minimum requirements for optimal system performance:

Windows

Processor:

Pentium II Processor

O/S:

Windows 2000, Windows NT, Windows 4.0 SP6a or Windows XP

Memory:

128 MB

Unix

Processor:

HP – HP9000/700 series

Sun – UltraSPARC 5

O/S:

HP – HP-UX 10.20 or 11.0

Sun – Solaris 2.6, 7 or 8

Memory:

256 MB

To learn more about how Tau can help improve your system verification process, call Mentor Graphics to schedule a complete product demonstration, or visit our website at www.mentor.com/pcb for the latest product news.

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