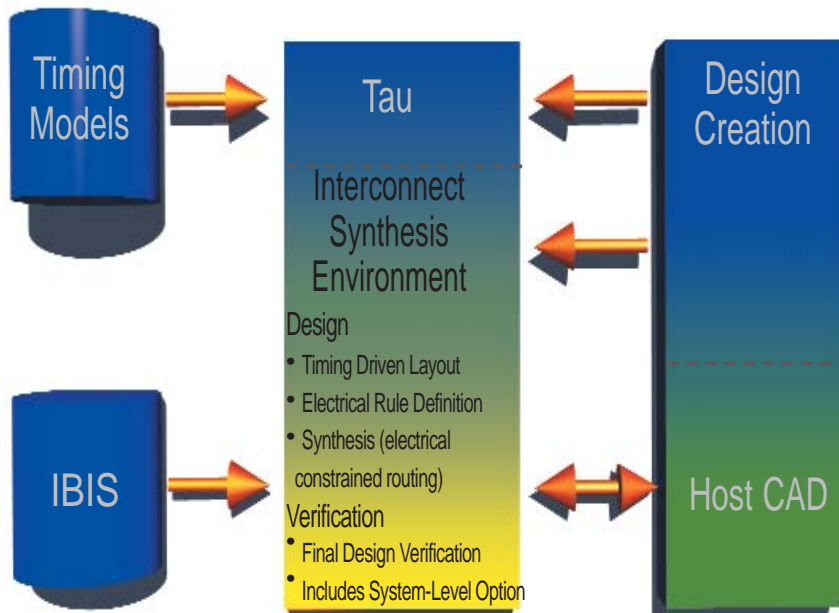


# Interconnect Synthesis (IS) Overview

D A T A S H E E T



## Major product benefits:

- A single integrated environment for design and verification of electronic systems
- Easy-to-use hierarchical rules management system
- What-if capability for developing rules, validating models and exploring design trade-offs prior to detailed design
- Timing-driven, hierarchical placement
- Electrically-driven routing process (Interconnect Synthesis)
- Full board or system-level design verification across all corner cases
- An extensive IBIS modeling solution with supplied models from Mentor Graphics
- Interfaces with most popular CAD systems

The Interconnect Synthesis (IS) family of products provides an advanced design and verification environment for even the toughest high-speed challenges. By integrating physical design with electrical verification, IS products provide a single environment for rules entry, what-if design exploration, timing-driven placement, electrically-driven routing and system verification.

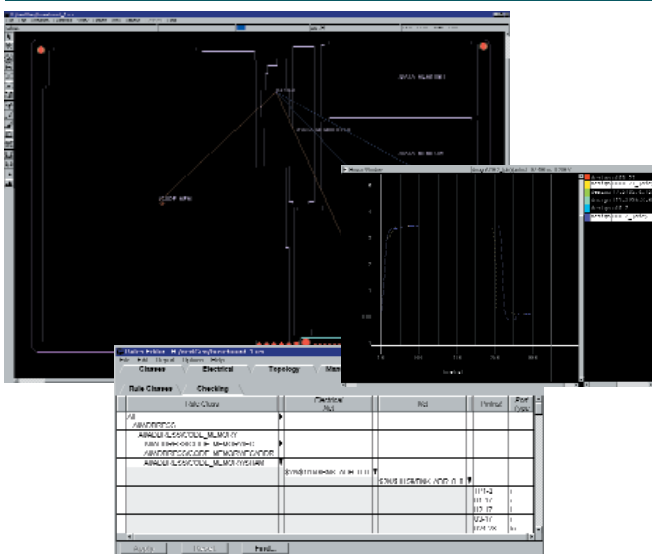
### Hierarchical Rules Entry and Management

The IS products leverage the power of a true hierarchical rules entry and management system. An interactive spreadsheet interface enables easy and effective management of both physical and electrical rules, which can be applied at both the class and net level.

Electrical requirements are specified in their native electrical terms and there is no translation of these into arbitrary physical constraints. The integration of this sophisticated rules entry system enables true concurrent constraint management.

### Analysis and Verification

The IS products feature an integrated parameter extraction module and a multi-conductor transmission line simulator. Components are modeled using industry-standard IBIS models. Results from simulation are used to drive all aspects of the design process, from early what-if analysis, to placement and routing, as well as full board and system verification.



*IS\_Floorplanner provides hierarchical, timing-driven floorplanning, graphical and spreadsheet-based interfaces and automatic simulation.*

Corner cases are defined in order to evaluate best and worst case scenarios. Accurate delay results are produced with simulation including pushout effects of crosstalk. Frequency dependent losses, such as dielectric loss and skin effects, are also modeled. The simulation resolution is controllable at the class and net level to one picosecond of accuracy.

### A Complete What-if Analysis Environment

The IS products enable pre-schematic what-if analysis by exploring and testing various design options. Vary topology, termination, driver selection, placement, board stackup, characteristic impedance and routing, to determine the optimum design implementation.

### Hierarchical, Timing-Driven Floorplanning

The IS products use the power of true, hierarchical placement to greatly simplify the placement process. Hierarchy is derived from the original schematic. This allows graphical manipulation of blocks of logic at any level of hierarchy. Additionally, background analysis provides continuous feedback during floorplanning, indi-

ating the ability to meet the electrical requirements.

### Electrically Driven Interconnect Design

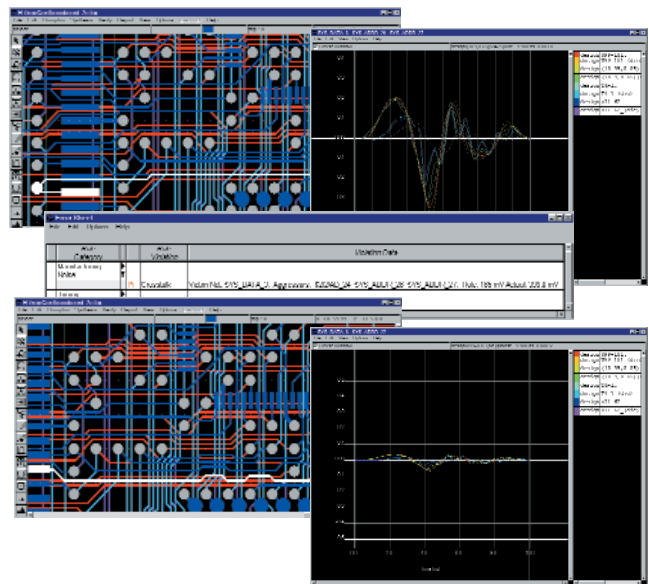
The IS products provide the capability to route a design to true electrical requirements. Simultaneous routing and simulation of delay and noise is carried out to produce a design that is both electrically and physically correct.

### Comprehensive Verification

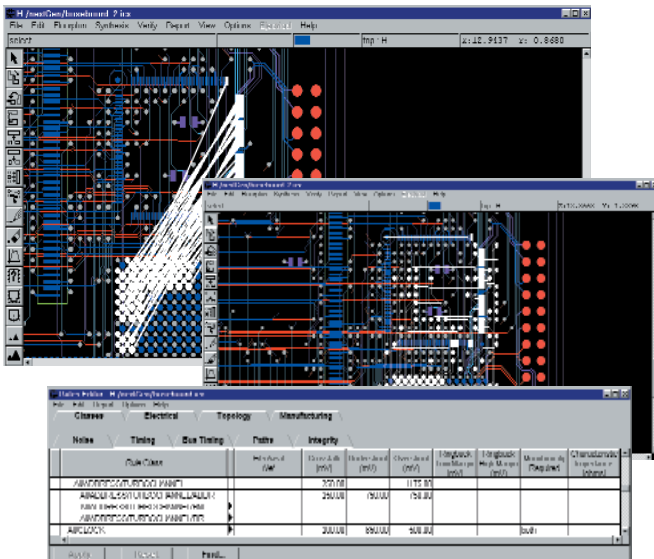
Using the IS products, full board or system level verification can be performed at any stage of the design cycle. The power to enter rules via the interactive spreadsheet interface, combined with the powerful analysis capabilities of the simulator, provides efficient system verification across all operating conditions.

### Integration with Tau

Tau<sup>fi</sup>, the Mentor Graphics board-level timing and analysis tool, can be used to generate delay constraints for the IS products. Net and bus level constraints entered in this way are used by the timing-driven placement and synthesis processes.



*IS\_Optimizer uses the powerful synthesis technology to automatically update designs to meet true electrical constraints.*



### IS\_Synthesizer

- Complete routing environment
- Simulations are run simultaneously during routing to ensure that designs meet electrical requirements

### IS\_Optimizer

- Use the interconnect synthesis technology to route critical nets to electrical requirements
- Electrically optimize routing created in a physically constrained environment

### IS\_Analyzer

- Full design and system level verification
- What-if environment for optimizing design trade-offs, including topology, termination, driver and stackup

IS\_Synthesizer offers a unique combination of real time analysis and routing that automatically generates net topologies that satisfy the design's true electrical constraints.

Simulation results for the interconnect delays can be back annotated to Tau at any stage of the design for timing verification.

### Interconnect Synthesis Products

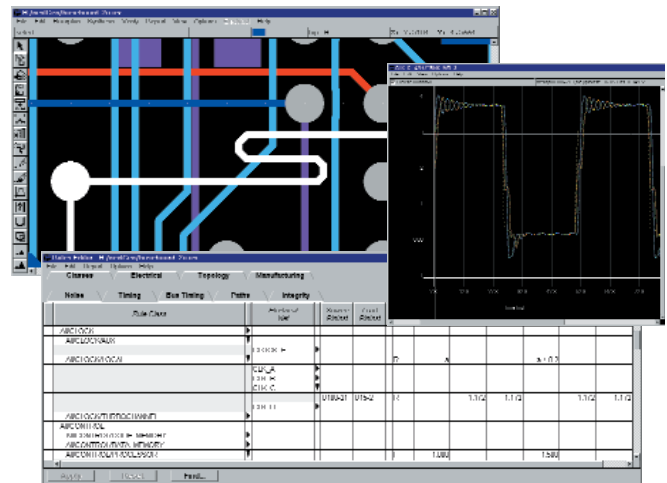
All IS products share the same design environment, rules entry and management system, integration with Tau, and transmission line simulator. Functionality is provided within individual products as described below. For more information, see individual product datasheets.

### IS\_Floorplanner

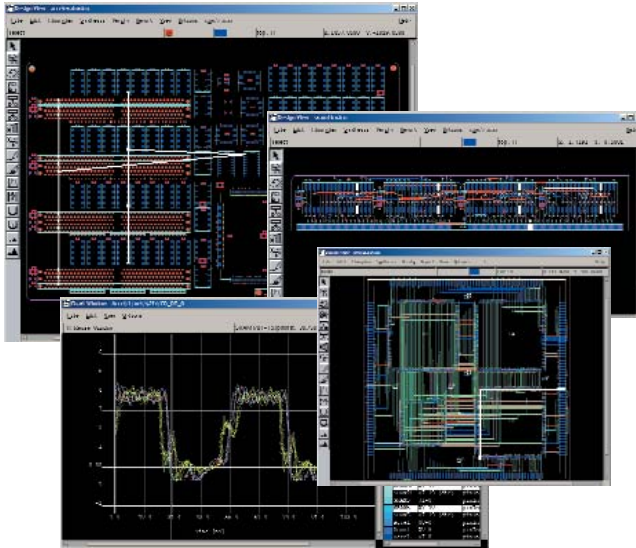
- Complete what-if analysis environment
- Hierarchical, timing-driven floorplanning
- Single net synthesis
- Full design verification

### IS\_MultiBoard

- Extends the powerful simulation and verification capabilities to the system level
- Uses SPICE-like format to model the system interfaces



IS\_Analyzer simulates nets and performs complete verification from a physical design, considering all timing and noise rules in either pre or post route phases of the design process.



*IS\_MultiBoard integrates multiple designs and provides simulation across the entire system.*

## Minimum Requirements

Mentor Graphics recommends the following minimum requirements for optimal system performance:

### Windows

Processor: Pentium II<sup>fi</sup> Processor  
 O/S: Windows NT<sup>fi</sup>, Windows 4.0<sup>fi</sup> SP6a  
 Memory: 128 MB

### Unix

#### Processor:

HP HP9000/700 series  
 Sun UltraSPARC 5

#### O/S:

HP HP-UX 10.20 or 11.0  
 Sun Solaris 2.6 or 2.7

Memory: 256 MB RAM recommended

To learn more about how the IS family of products can help improve your high-speed board design process, call Mentor Graphics to schedule a complete product demonstration, or visit our website at [www.mentor.com/pcb](http://www.mentor.com/pcb) for the latest product news.

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