

HyperLynx GHz includes a complete suite of tools for pre- and post-layout signal integrity, crosstalk and EMC analysis, including multi-gigabit per second SERDES interconnects.

## Major product benefits:

- Industry leading ease of use
- Accurate modeling of lossy transmission-line effects, including skin effect and dielectric loss
- Analyze inter-symbol interference in multi-gigabit signals, including random jitter, eye diagrams, and eye masks to define keepout regions
- Simulate with SPICE or IBIS models
- Advanced via modeling
- Differential signal simulation and analysis, including impedance planning and optimization of differential terminations
- Terminator Wizard™ recommends optimal termination strategies, including series termination, parallel, parallel AC, and differential
- Provides an early look at likely EMC failures, including both radiation and trace current analysis
- Works with all major PCB layout and routing applications

## Overview

Increasingly fast edge-rates in today's integrated circuits (ICs) cause detrimental high-speed effects, even in PCB designs running at low operating frequencies. As driver ICs switch faster, a growing volume of boards suffer from signal degradation, including over/undershoot, ringing, glitching, crosstalk, and timing problems. When degradation becomes serious enough, the logic on a board can fail-making otherwise excellent designs stare blankly into space.

HyperLynx® EXT — including LineSim™ for pre-layout analysis and BoardSim™ for post-route analysis — targets designs at frequencies up to about 300 MHz. At higher speeds, transmission-line losses (including skin effect and dielectric loss) and via parasitics take on increasing importance; the HyperLynx GHz bundle models all of these effects and addresses the special needs of SERDES design.

## Complete SI and EMC Analysis Suite

Signal integrity and timing analysis, for most engineers, is only one of many systems design tasks. A software tool that's easy to learn and easy to relearn is a necessity with today's schedule pressures.

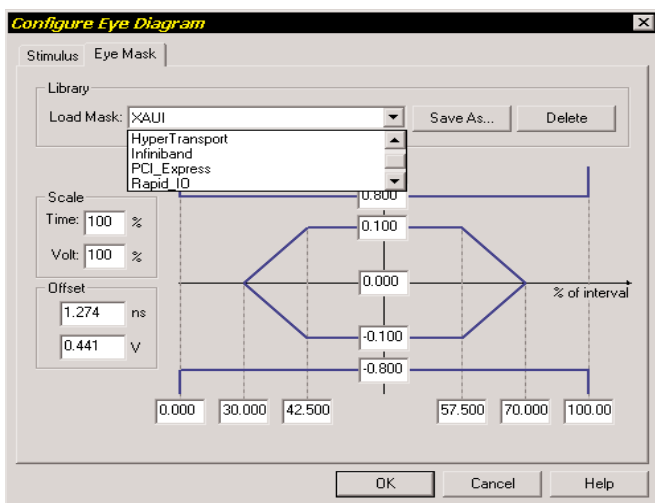
Hardware engineers, PCB designers and signal integrity specialists alike can use HyperLynx as a team; getting simulation results without requiring weeks of software training. The emphasis is on getting designs right the first time, avoiding costly overdesign, and saving recurrent layout, prototype and test cycles in the lab.

With HyperLynx, you can address high-speed PCB problems throughout the design cycle, beginning at the earliest architectural stages and moving through post-layout verification. The process is as easy as using an oscilloscope or spectrum analyzer in the lab, and at a fraction of the cost.

## LineSim GHz

Pre-layout simulation with LineSim GHz, part of HyperLynx GHz, allows you to predict and eliminate signal integrity problems early, allowing you to proactively constrain routing, plan stackups, and optimize clock, critical signal topologies and terminations prior to board layout. LineSim's intuitive drag-and-drop transmission-line modeling approach is an ideal way to "get it right" the first time.

- Quickly enter complex interconnect scenarios, including ICs, transmission lines, cables, connectors and passive components
- Simulate immediately, using industry-standard IBIS models, HyperLynx's 18,000 model IC library, generic models, or build your own models from databook information
- Visual IBIS Editor allows you to check and edit IBIS models including a hierarchical, newer, automated syntax checking V/I-V/t auto-correction and drag and-drop curve editing
- Easily instantiate and simulate HSPICE or Eldo models (SPICE software sold separately)
- Start from scratch or use one of the design kits for Xilinx RocketIO, Altera Stratix-GX, PCI-X, USB and more



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## BoardSim GHz

Post-layout signal integrity simulation with BoardSim GHz, part of HyperLynx GHz, allows you to analyze signal integrity and timing at three important stages: following part placement in your PCB layout system, after critical net routing, and after detailed routing of an entire board.

- Batch simulation automatically scans large numbers of nets on an entire PCB, flagging SI and EMC hot spots
- Interactive analysis takes you to the next level, simulating batch analysis-identified trouble spots
- Quick Terminators allow new termination components to be inserted on-the-fly, enabling real-time analysis
- Accurately predicts crosstalk waveforms for any trace topology and IC placement, also showing board designers specific cross-sections in violation of crosstalk thresholds
- Powerful, easy to use multi-board analysis, including support for EBD models

### BoardSim-compatible PCB layout systems:

- Mentor Graphics PADS® Layout, Expedition™ and Board Station®
- Cadence Allegro, SPECCTRA and OrCAD Layout
- Altium Protel and P-CAD
- Intercept Pantheon
- Zuken CADStar, Visula and CR3000/5000 PWS or Board Designer

## Minimum Hardware/Software Requirements

### Windows XP or 2000

- Pentium II 333 MHz CPU, or faster
- 128 MB RAM; 60 MB hard disk space
- 1024 x 768, 256 color display
- NIC, Parallel port, or USB port to supply HostID to license management software
- 165 MB for Extended IBIS Libraries

### Sun Solaris™ version 8 or 9:

- 320 MB hard disk space
- 165 MB for Extended IBIS Libraries

### Recommended patches for Solaris 8:

- Recommended Patch Cluster: March 19, 2002 or later
- Mach 64 Graphics card patch: 108606-31 or later

To learn more about high-speed design and HyperLynx software, visit [www.mentor.com/hyperlynx](http://www.mentor.com/hyperlynx) to download the high-speed design tutorial, or call to schedule a product demonstration.

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