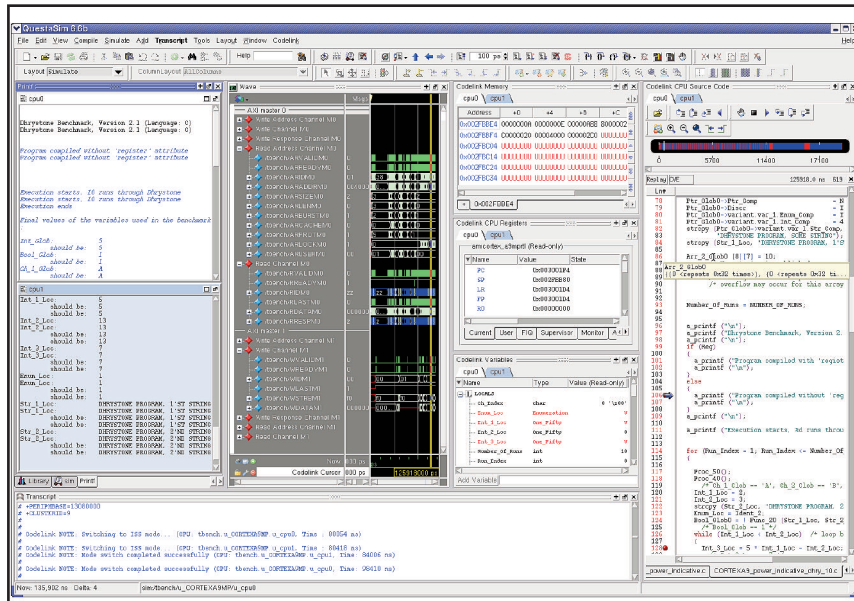


# Questa Codelink-CVE®



*Questa Codelink-CVE accelerates software instruction execution and provides full processor(s) debug visibility for more efficient SoC debugging and verification.*

## Overview

Today's SoC projects include embedded processors and must deliver working embedded software and hardware. Identification of critical hardware/software integration issues early in a project can avoid painful, time-consuming, schedule-eating defects that can derail a project's timeline or jeopardize the project's quality. Using the Questa Codelink® CVE solution, embedded software and physical hardware arrive at system integration already having been run together. Many defects at the hardware/software junction have already been fixed so the project can progress quickly on the hardware prototype. Codelink CVE gives you confidence and reduces the risk of project failure.

Codelink-CVE stands for Co-Verification Environment. The tool delivers speed, full visibility and control of your ARM, MIPS, and IBM PowerPC processors while running your entire SoC design using an HDL logic simulator. By executing embedded software on HDL-simulated hardware, Codelink CVE allows you to accurately debug and verify hardware/software interactions before a hardware prototype is available. Eliminating defects in the hardware/software interaction provides product quality while preserving or even accelerating the project schedule. You gain confidence that the complete product works – both the hardware and the software – early in the project before a hardware prototype is available. Codelink CVE's ability to run in sign-off accurate mode or fast, high performance, software execution mode, and to dynamically switch between the two under your control, enables you to execute significant amounts of software while retaining the fidelity of your logic simulation environment.

## Major product features:

- Fast ARM, MIPS, and IBM PowerPC debug visibility in HDL logic simulations
- Live and Replay mode for interactive post-simulation debug
- Software source code and hardware waveforms are fully synchronized
- Multi-core support
- Step forward or backward through source or assembly
- Source, assembly, memory, variable, register, call-stack and standard output views
- Four level logic (0, 1, U and X) in the software debug windows
- Dynamic switch between cycle (RTL) and instruction (ISS) level of processor's simulation accuracy
- TLM interface and Host Mode support

## Major product benefits:

- Speed software execution in simulation
- Debug multi-core synchronization errors
- Replay overnight batch simulation in seconds
- Radically reduces debug time for tests using processors
- Allows RTOS boot-up in HDL simulation

## Overview (cont'd)

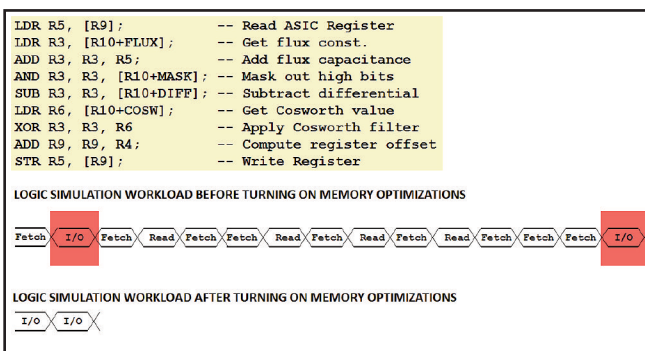
In sign-off cycle accurate mode (RTL), an existing processor model at RTL or DSM (Design Simulation Model) level runs the embedded software. The instruction accurate mode uses a fast instruction set simulator (ISS) connected to a Bus Functional Model to run the embedded software. No software changes are required.

Codelink-CVE comes with predefined processor wrappers instantiating both RTL and the fast ISS models along with the switching mechanism allowing users to propagate states back and forth between the fast ISS and RTL model. Significant CPU instruction per second acceleration is achieved when running with the fast ISS model. Codelink-CVE fast ISS models run 100,000 times faster than RTL or DSM models.

Two modes of operations are supported: Live and Replay. The Live mode provides visibility and control of the processors and embedded software while running HDL simulation. During Replay mode, Codelink-CVE reads a processor execution trace data file so you can debug the design post-simulation. In both modes software code and hardware waveforms are fully synchronized.

## Codelink-CVE Speeds Simulation

The acceleration mechanism relies on fast processor simulation models reduces the need for redundant HDL simulator cycles by removing all HDL simulation cycles used for accessing memory to fetch instructions or read and write data. The technology uses coherent memory servers that are accessible both by the fast ISS and the logic simulator to eliminate HDL simulator cycles used for hardware memory accesses. This process is called memory access optimization since the number of bus cycles between CPU and memories as HDL simulation events is reduced to only I/O operations.



The memory access optimization is highly interactive allowing you to control which address spaces need to be mapped to coherent servers to on or off logic simulation transactions. Thus, the ratio between HDL simulation speed and debug visibility is fully scalable.

## The Host Mode

The Codelink-CVE Host Mode of operation enables you to run simulation on embedded software you compile and execute on your workstation. Since you are using embedded software executing on your workstation, simulation runs much faster than if you were using target code executing on a software simulator. Portions of your embedded software can even be implemented in a high-level language and tested directly with the logic simulation, without having target code available. You can use the native compilers on your workstation to develop your embedded software.

## Hardware Defect Diagnosis

HDL logic simulators are not designed for debugging embedded CPUs. Debugging a full functional processor model when it goes into “flat-line” becomes a challenging task. The design simulation models for processors provide instruction trace files (EIS – Executed Instruction Stream, Tarmac – Trace ARM Accesses, MIPS – trace, etc.) which include a list of fatal errors while the waveform shows no processor pins activity for a number of clock cycles. Relying on these two simulation outputs exclusively can be very tedious and cumbersome.

Codelink-CVE increases the debug productivity of SoC verification by monitoring the register changes of processor models from ARM, MIPS, and IBM PowerPC and adding a software source viewer into the HDL simulation environment. Both source and assembly level embedded software are supported. Visibility is provided into software variables, processor registers, memory and stack, all of which update dynamically. The hardware waveform viewer cursor is synchronized with the software source window, thus the wave cursor tracks your progress as you step through the code. Likewise, dragging the waveform cursor will scroll the source view to the corresponding source line containing the instruction being executed. The breakpoint mechanism is supported as well.

Existing software debuggers lack comprehensive representation of X-states that are too common in HDL logic simulation. Codelink-CVE allows X-states to appear in register and memory windows.

The memory viewer provided by your HDL logic simulator shows only physical addresses. When simulating with local CPU caches turned on, some of the memory transactions can be hidden. On the other hand, turning off CPU caches slows down the entire simulation performance. Codelink-CVE memory viewer avoids these limitations by allowing you to see virtual addresses directly supporting both cache and memory management units.

## Interactive Post-Simulation Debug

There is no need to re-run failing regression tests in order to isolate the case of the failure. During simulation Codelink-CVE observes changes in the processor's general purpose registers and memories then saves the information to a replay file. After simulation Codelink-CVE loads the saved software replay file in conjunction with waveform file. The mechanism is highly interactive allowing you to move instantly to any point in the simulation record with full hardware/software debug visibility in a blink of an eye.

## Step Through Code in Reverse

Codelink-CVE has the ability to un-execute software code so you can step backward through your code. As you step, a cursor in the hardware waveform window simultaneously tracks the instruction execution.

## Dynamic Modification

In the Live and ISS simulation mode, you can change the values of registers, memory and software variables when HDL simulation is stopped. Advancing the processor to the next instruction will use new values allowing you to do what if analysis without software recompilation.

## Multi-Core Support

For multi-core designs, Codelink-CVE simultaneously monitors multiple processors. Any mix of supported processors can be logged during a single simulation. The Codelink-CVE graphical user interface presents source, memory, register, variable, and call stack windows for each core in the design. The user can choose tabbed, tiled, vertical or horizontal window orientation.

## Standard Software Output Console Support

The software *printf* function sends a message to a standard IO which then prints it in the UART or to the logic simulator terminal window consuming multiple simulation clock cycles. Codelink-CVE standard output window allows displaying software *printf* messages consuming almost 0 clock cycles.

## TLM Interface

Codelink-CVE instruction set simulator models provide both a SystemVerilog and a SystemC TLM (Transaction Level Model) interface. The SystemVerilog TLM interface is compliant with OVM 2.0.2 and 2.0.3. The SystemC TLM interface is compliant with TLM 2.0. The TLM interface can be used in mixed language designs to communicate with the SystemVerilog or SystemC portions of the design at a transaction level. The TLM interface is supported in instruction accurate (ISS) mode only.

<i>Supported Processors</i>				
ARM			MIPS	IBM PowerPC
7TDMI	1136	Cortex-R4F	4KE	PPC405
7TDMI-S	1156	Cortex-A5	M4K	PPC440
926	1176	Cortex-A8	24K	Virtex5 (PPC440)
946	Cortex M0	Cortex-A9	24KE	
966	Cortex M3	Cortex-A9 MPCore	74K	
968	Cortex R4			
<i>Supported Platforms and Logic Simulators</i>				
Red Hat Enterprise Linux 4 for 32-bit and 64-bit				
Red Hat Enterprise Linux 5 for 32-bit and 64-bit				
Mentor Graphics ModelSim <sup>®</sup> , Questa <sup>®</sup>				
*Cadence Incisive Enterprise Simulator (logging processor states only)				
*Synopsys VCS (logging processor states only)				
<i>*ModelSim/Questa viewer license required for interactive post-simulation debug</i>				
<i>Supported Third Party Tools</i>				
Hardware debugger: SpringSoft Verdi Automated System				
Software debugger: ARM Workbench IDE in RealView Development Suite				

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